SEL-451 MOTOR BUS TRANSFER SVEC USER GUIDE



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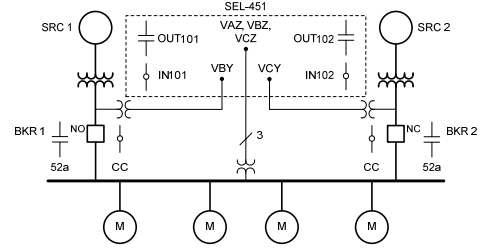
11/19/2015 – REV 1

# INTRODUCTION:

The SEL-451 has many uses for Protection, Automaton, and Bay Control Systems. Here at SVEC we are implementing a base version of SEL’s application guide Volume VIII AG2012-01 “Motor Bus Transfer Scheme for a Two-Source Configuration Implemented in the SEL-451”. We have made some modifications to the original SEL program. For the most part these settings are used to implement a two-source configuration, this whitepaper will provide an overview of the logic and settings scheme to help in aid of understanding and troubleshooting.

# BACKGROUND:

This scheme is set up so that monitoring on the motorbus can be used to safely automatically transfer the load from one source to an alternate in the event of a fault.



## Figure 1: SEL’s illustration of a single-line diagram

For more clarification on the figure above, each source has a single PT that is reporting from the B phase to the 451. The motor bus has a PT for each phase reporting to the 451.

In this case shown the SRC2 breaker is feeding the motorbus. In our application we have a preferred source that can be selected while the motor bus may be energized from either source, we can select one that we feed from based on our custom logic.

# TRANSFER MODES:

Three modes come standard in this scheme, they can be set so that as the motor bus voltage drops in magnitude and frequency the 451 can have multiple attempts to transfer the load to the other source.

## Fast Bus Transfer:

When enabled the fast mode has 2 types of fast transfer to select from, simultaneous and sequential. This mode is the very first mode to attempt the transfer when it is enabled.

In simultaneous transfer, as the present source breaker opens, the alternate source breaker closes. SEL doesn’t guarantee that both breakers will not be closed at the same time, this is a risk that will have to be evaluated before implementing this mode. This mode would also require a 52b input into the 451 for breaker position confirmation.

Sequential transfer is the other fast bus mode, this logic insures that the present source breaker is open before sending the close to the alternate source breaker. SEL uses the aid of current in their logic, here at SVEC we modified our settings to only use the 52A contact. If we implement these settings the 52B contact should be connected to the 451 for breaker confirmation.

SEL says Fast Bus transfer is most appropriate when both sources come from the same phasing, and that a synchronism-check element should be implemented before the transfer is enabled.

## In-Phase Transfer

In-phase transfer mode comes into play after the trip has already been initiated and both breakers are in the open position. At this instance the motor bus voltage is decaying in magnitude and in frequency, this can vary based on the back EMF of the motor load on the system. If enabled the in-phase mode will begin after the fast transfer mode. SEL has devised some logic that will calculate motor slip which is the frequency difference in the motor bus and the transferring source voltage. Using the close time of the breakers in the settings the 451 can send the close signal while predicting the best instance to close into the decaying frequency of the motor bus.

In this mode many things are checked before issuing the close. This includes the slip frequency between the source and motor bus; the slip frequency change over time; the motor bus voltage magnitude; and the motor bus voltage magnitude change over time. \*\*If we implement this we must learn what the protection bit PSV01 does in the logic and re-implement it, where it is commented out of the logic. During tests we couldn’t get the breaker to reclose with this bit in the logic.\*\*

## Residual Transfer

Residual transfer is the situation that has both breakers open and waits for the magnitude of the motor bus voltage to drop below a desired level. At this point the phase and frequency are so low that closing into the alternate source should not damage the machines or motors in anyway. \*\*At this point 11/13/2014 we only have the Residual Transfer Mode enabled.\*\*

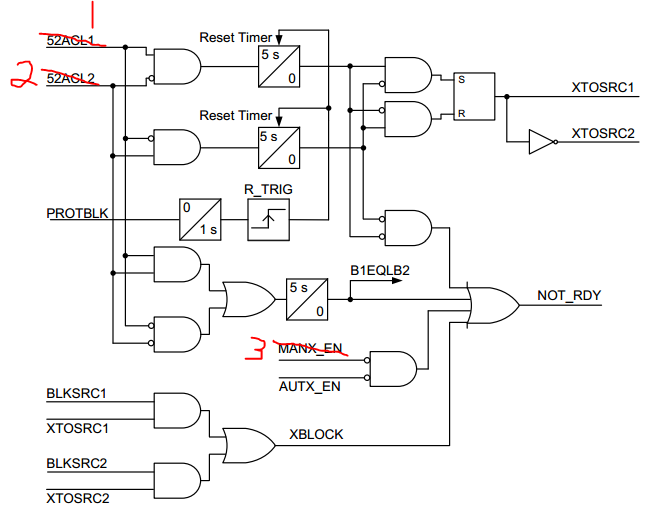
# SOURCE SELECTION

The PT’s that are monitoring our two sources are using the B Phase of each source. While our gear has PT’s on all three phases of the two sources for this scheme we are only implementing the use of the A Phase PT’s (as of 3/4/2015). These are wired into the 451 after landing on some terminal blocks, with source 1 connected to VBY and source 2 connected to VCY.

SEL logic at this point has been modified and I will indicate the changes and describe them in detail.

The changes for 1 and 2 are both based on the 52ACL1 and 52ACL2 using current as a verification of breaker status, we decided to go with the inputs of our breakers. This was replaced in our settings with IN205 for 52ACL1 and IN206 for 52ACL2, these inputs are wired into the 52A contacts that follow the breakers status.

Change 3 is where we completely removed the manual portion of the SEL logic. So it does not exist.



## Figure 2: source selection logic showing SVEC modifications

# PUSH BUTTONS

## Table 1: Pushbuttons Labels and Descriptions



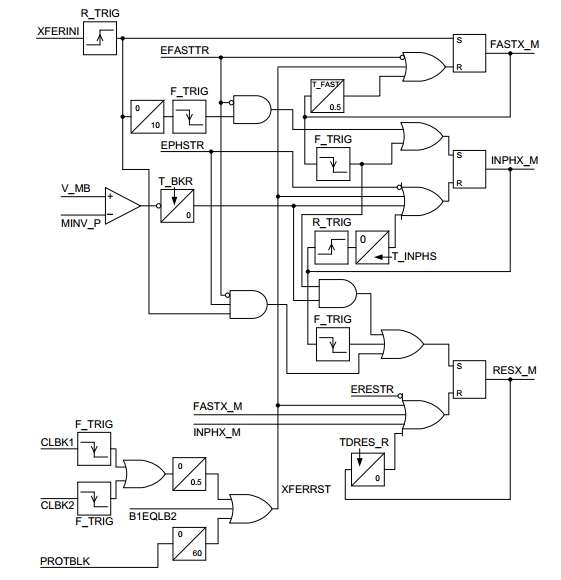
# TARGET LEDs

## Table 2: Target LEDs Labels and Descriptions



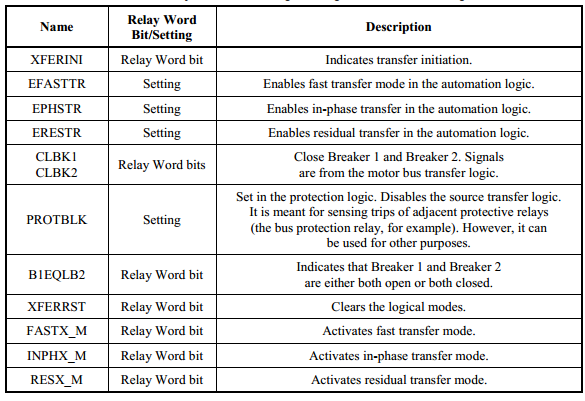
# TRANSFER MODE LOGIC

From the SEL Application Guide, when the SEL-451 enters a transfer sequence, it will initiate fast, in-phase, or residual mode. This is depending on which modes are enabled, once in the mode the logic has a time window set to get certain criteria met before issuing a close signal. If the criterion isn’t met then the logic will go to the next transfer mode (Fast, in-phase, residual depending on where the sequence began) or, it will out put a failed transfer signal. As soon as a mode sends a close command it resets the logic in the SEL-451, another XFERINI must be sent.

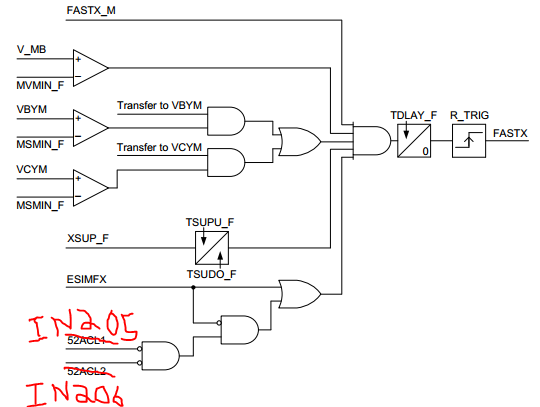


## **Figure 3: SEL Transfer Mode Logic Diagram**

## Table 3: SEL Relay Word Bits and Logic Settings for Transfer Mode Logic

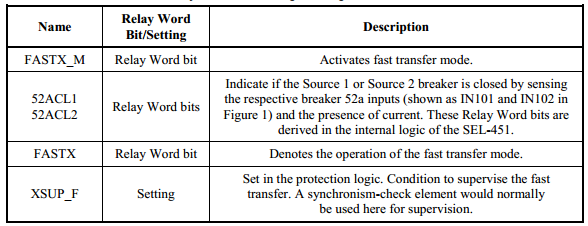


# Fast Transfer Mode

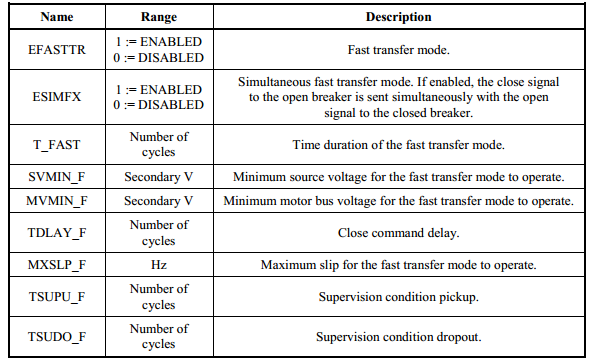
Fast transfer mode has 2 sequences. The sequential transfer where the opening of the closed breaker is verified before the close signal is sent. Then the simultaneous sends the trip and close signals at the same time. You can see that this is governed by the Relay Word Bit ESIMFX and the and gate at the bottom of figure 4. Again remember that the 52ACL1 was replaced with IN205 and 52Acl2 was replaced with IN206.

## Figure 4: Fast Transfer Mode Logic

## Table 4: Fast Transfer Mode Logic Relay Word Bits and Logic Settings

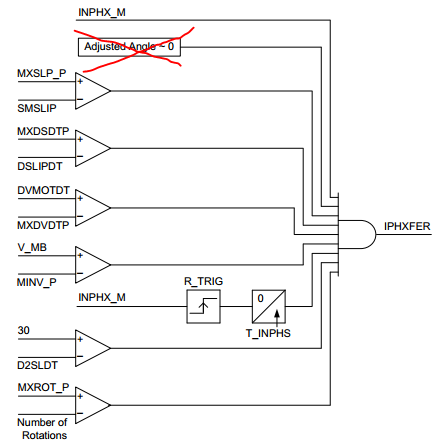


## Table 5: Fast Transfer Mode Settings



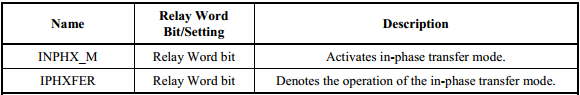
# In-Phase Transfer Mode

The in-phase transfer mode issues the close assuming the rate the slip is changing along with the operating time of the breaker in order to close near a zero angle difference when the breaker contacts close. We were having trouble with the Adjusted Angle ~0 (PSV01 in the logic) so we removed it from our test set up, we will need to preform tests on this before implementation.

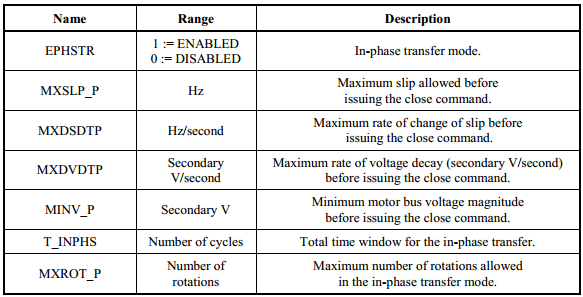


## Figure 5: In-Phase Transfer Mode Logic

## Table 6: Relay Word Bits for In-Phase Transfer Mode

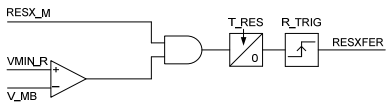


## Table 7: In-Phase Transfer Mode Settings



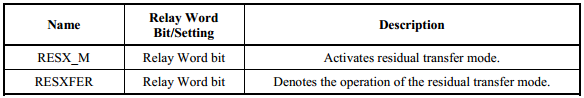
# Residual Transfer Mode

This is the mode that we will begin with until we get enough data and contractual agreements to try for the more risky Fast and In-Phase modes. The Residual Transfer Mode has a single check and a delay for security. This mode assumes that the load is still rotating and the motor bus voltage has decayed to below 20 volts on the secondary side of the Power Transformer’s on the motor bus. This is slightly higher than the default from SEL of 15 volts; we raised it due to a static voltage on our secondary wiring. We have our T\_RES=120.00 cycles, to give a 2 second delay after the voltage minimum is met.

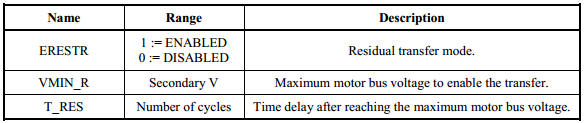


## Figure 6: Residual Transfer Mode Logic

## Table 8: Residual Transfer Mode Relay Word Bits

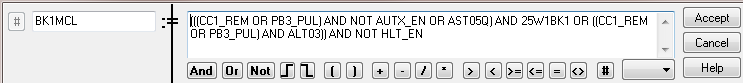


## Table 9: Residual Transfer Mode Settings



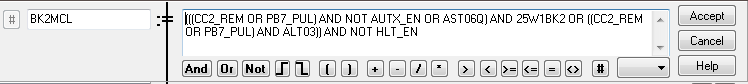
# Close Equations

Below Figure 7 shows the close equation for breaker 1 “KR25W1”. The CC1\_REM takes the remote close command anded with the remote enable in the protection logic. This is ored with the PB3\_PUL which is the pushbutton designated to close KR25W1, all of these are and notted with AUTX\_EN, this makes sure the auto transfer scheme is off when trying to close by remote or locally. This is also ored with AST05Q. AST05Q is the preferred source close timer for KR25W1, the preferred source is set in the automation logic and requires the voltage to be present for 15 minutes before preforming a closed transfer back to the preferred source. \*\*\*As of 12/2/14 this is source 1 this is set by, ASV024 := 0\*\*\* This first section is governed by the sync checking done by 25W1BK1. The second section contains the remote and local closes ored together and anded with ALT03. ALT03 is a latch created in the automation logic to allow for dead bus – live line and live bus –dead line closing. With the entire close command governed by NOT HLT\_EN to ensure safety while hot line tag is enabled.



## Figure 7: Close Equation for Breaker 1 “KR25W1”

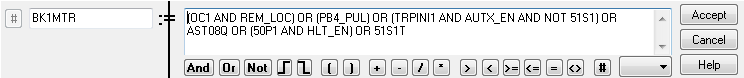
The close command for breaker 2 “KR25W2” is just like the one for breaker 1 with its corresponding variables. See figure 8 for details.



## Figure 8: Close Equation for Breaker 2 “KR25W2”

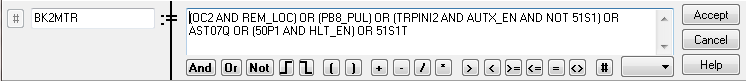
# Trip Equations

Below figure 9 shows the trip equations for breaker 1 “KR25W1”. The Logic here begins with OC1 anded with REM\_LOC, this is the remote open anded with the remote enable. This is ored with PB4\_PUL, the pushbutton that is designated to open KR25W1. This is ored with TRPINI1 AND AUTX\_EN AND NOT 51S1, the TRPINI 1 is logic developed in the protection logic which initiates the trip when the motor bus voltage is less than 20 volts, and the alternate source has a voltage between 108 and 132. This is anded with AUTX\_EN so that this trip only happens when auto transfer is enabled. The AND NOT 51S1 is there to make sure the TRIPINI1 doesn’t initiate a trip when the current levels have the time overcurrent picked up. Then the OR AST08Q comes in as the trip part of the closed transfer of the preferred source scheme. Everything is ored with the 50P1 AND HLT\_EN to trip the breaker for an instantaneous current higher than the limits set when the hot line tag is enabled. Lastly everything is ored with 51S1T which is the time overcurrent timeout.



## Figure 9: Trip Equation for Breaker 1 “KR25W1”

Again breaker 2 “KR25W2” is the clone of breaker 1 with its own variables, shown in figure 10.



## Figure 10: Trip Equation for Breaker 2 “KR25W2”

# Inputs

## Table 10: Inputs



# Outputs

## Table 11: Outputs

