Motor Bus Transfer Scheme for a Two-Source Configuration Implemented in the SEL-451

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INTRODUCTION

The SEL-451 Protection, Automation, and Bay Control System has extensive logic and protection features, allowing it to be used for many applications. This application guide describes how to implement a motor bus transfer scheme in the SEL-451 for a two-source configuration. It begins by providing an overview of motor bus transfer and the three common modes of transfer. The application guide then provides an overview of the logic and settings scheme to help in understanding the logic and settings. The guide then covers an application where settings are provided for an example system. Finally, example event reports illustrating the logic and settings are discussed.

An ACSELERATOR QuickSet® SEL-5030 Software settings file that contains the logic described for the SEL-451 is available with this application guide at http://www.selinc.com. Consequently, using the example settings file when reviewing the guide is recommended. Because SELOGIC® control equations are used to implement the interlocks, additional customization can be performed if needed.

BACKGROUND

When a three-phase source is disconnected from a motor bus, the load attached to the motors keeps rotating and deaccelerating, while, at the same time, the motor bus voltage decays both in frequency and in magnitude. In the electric power industry, a source transfer scheme is used to automatically transfer the motor bus to an alternate source.

Figure 1 illustrates the single-line diagram used to describe the problem and the application in this guide.

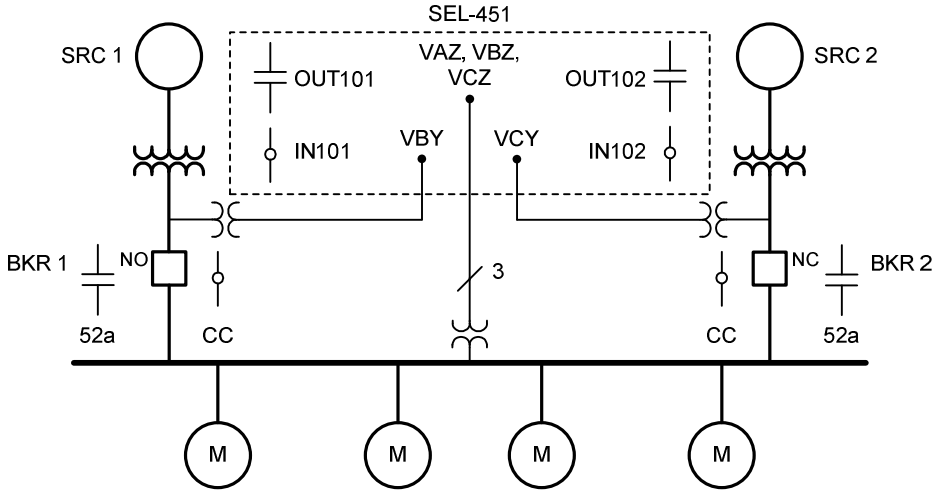

Figure 1 Source Transfer Scheme

In Figure 1, the motor bus is operating from Source 2 (SRC 2) initially. If Source 2 is lost and isolated by manual or protective relaying actions that open the normally closed (NC) Breaker 2 (BKR 2) and if Source 1 (SRC 1) is available, the motor bus should safely and rapidly be transferred to Source 1 by closing the normally open (NO) Breaker 1 (BKR 1). Similarly, if operating conditions are such that the initial source is Source 1, then the transfer involves sending the close command to Breaker 2. The scheme implemented in the SEL-451 contains the necessary logic and measurements to send a close command (OUT101/OUT102) to the close coil (CC) for Breaker 1 (or Breaker 2) to accomplish a motor bus transfer.

Relay Selection

The transfer scheme is implemented in the SEL-451. There is a variety of ordering options available for the SEL-451. The inputs and outputs in the base model and the required additional inputs and outputs needed to implement the scheme described in this application guide are as follows:

- The SEL-451 base model comes with eight digital outputs and seven digital inputs (three high-current, two standard Form A, and three Form C digital outputs and seven level-sensitive optoisolated inputs).
- The scheme requires high-speed, high-current output contacts for the closing signal to the Source 1 and Source 2 breakers. This means having at least one I/O board with high-speed, high-current output contacts.

Other ordering options not described are not critical to the motor bus transfer logic outlined in this application guide but, of course, must be considered when selecting the part number for the SEL-451.

The hardware in the SEL-451 should include high-speed output contacts for the close signals. The compensation angle for the in-phase transfer mode should be based solely on the breaker time. The close command output contact should not introduce additional time such as the SEL-451 traditional output contact operating time. The operating time of the high-speed contacts is negligible and can be disregarded.

Motor Bus Voltage Behavior

The scheme is challenged by the behavior of the motor bus voltage when the source is lost. Source transfers should be executed to ideally conserve the phase, magnitude, and frequency of the original source. After a disconnection from its source, the voltage at a motor bus decays both in frequency and in magnitude, making the determination of a phase difference more difficult.

Figure 2 illustrates the magnitude and voltage decay for a motor bus after the main source is disconnected. The source voltage (VB) remains at a constant frequency and magnitude. A source transfer scheme should ensure source transfer within a reasonable phase difference, magnitude difference, and slip (difference between the source and the motor bus frequency).

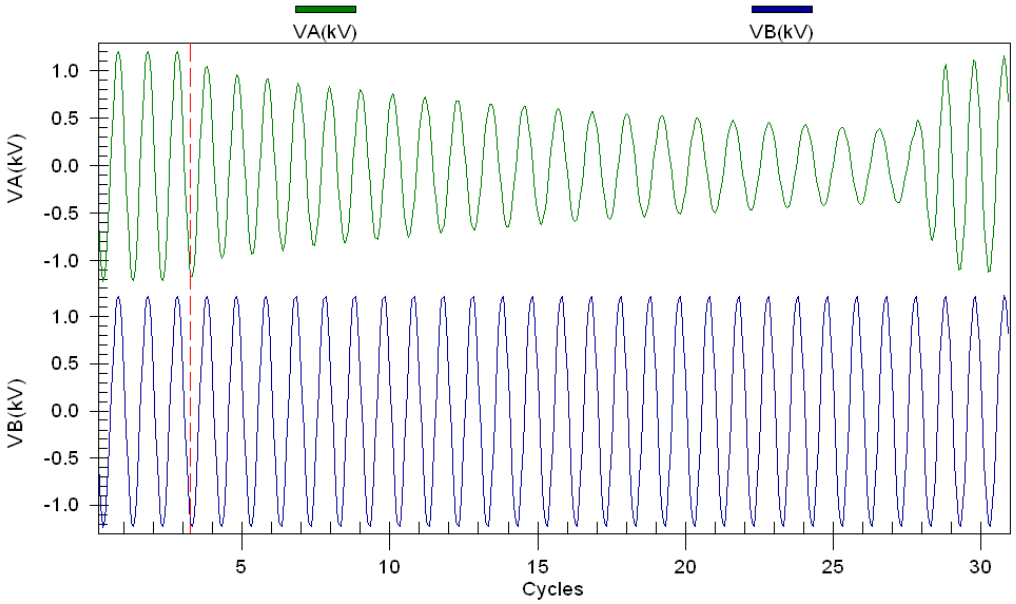

Figure 2 Motor Bus Voltage (VA) and Source Voltage (VB)

Transfer Modes

Three modes of motor bus transfer are generally recognized in the industry. Due to the decaying magnitude and frequency of the motor bus over time, these transfer modes can be defined over time. Certain criteria need to be satisfied in each mode to achieve the closure to the new source.

Fast Bus Transfer

The fast bus transfer mode, when enabled, is the first mode to operate because its duration starts from the moment the transfer has initiated. There are two types of fast transfers: simultaneous and sequential.

In a simultaneous transfer, as the present source breaker opens, the transfer source breaker closes. The logic does not guarantee that both breakers will not be closed at the same time if the present source breaker fails to open. An early transfer initiation signal is required, which generally is a fast 52b breaker position or the open command input.

In a sequential transfer, the logic ensures that the present source breaker is open, so then the close signal can be sent to the transfer source breaker. The logic ensures that both 52a breaker position inputs are not present and that there is no current, at the same time.

The fast bus transfer mode is appropriate when the two sources come from the same phasing. Usually, before entering the mode, a synchronism-check element ensures that the motor bus voltage and the transfer source are in phase.

In-Phase Transfer

The in-phase transfer mode assumes the two breakers are already open and the motor bus voltage is decaying both in magnitude and in frequency. In the SEL-451 scheme, the in-phase transfer mode, if enabled, starts after the fast transfer mode.

The transfer source will have steady nominal frequency and nominal voltage that both remain constant. The motor bus frequency and voltage magnitude will be decaying. Due to the frequency difference (slip) between the motor bus voltage and the transfer source voltage, there will be instances when both voltages are in phase. The in-phase transfer mode calculates in advance the minimum phase angle difference between the two voltages and issues a close signal based on the closing time of the alternate source breaker.

The internal logic checks several conditions before issuing the close command. The conditions include that the slip frequency between the motor bus and the source, slip frequency change over time, motor bus voltage magnitude, and the motor bus voltage magnitude change over time are all within specified limits. The important condition is the proper calculation of the time to issue the close signal, taking into consideration the conditions mentioned and the breaker closing time.

Residual Transfer

If the magnitude of the motor bus voltage has decayed significantly and only a small magnitude is left at any frequency, closing the alternate source breaker at any phase angle difference does not cause damage to the machine. Residual transfer is very similar to starting the motors connected to the bus simultaneously. When implementing a residual transfer, to avoid problems with starting all the motors on a bus simultaneously, certain motors may be tripped offline and restarted after the motor bus has been transferred. Evaluating whether all the motors on a bus can be started simultaneously and how to implement automatic restarting of these motors after such a transfer is beyond the scope of this application guide.

Because the residual transfer by definition assumes the motor bus voltage has decayed to a safe level to avoid damaging transient torques, the scheme, in essence, only requires a simple voltage check to verify that the motor bus voltage has dropped below a certain threshold. As such, it is the simplest and easiest to implement of the three transfer methods in terms of relay logic and relay settings.

Implementing Measurements and Source Selection in the SEL-451

The SEL-451 is ideal for installations that operate with a single frequency and with slow rates of change. To adapt the SEL-451 to the demanding problem of motor bus transfer, we need to disregard the native measurements for frequency and implement an algorithm that can truly measure the motor bus frequency as well as the source frequency.

The firmware of the SEL-451 is designed for feeder applications, and the measurements and logic (specifically for the synchronism-check function) are too slow for motor bus transfer applications. Customized logic in SELOGIC control equations is used to implement needed measurements for motor bus frequency and needed quantities for the transfer modes, in addition to the transfer logic, which is discussed later in this application guide.

Refer to Figure 1, where the voltage inputs are described. The source (1 or 2) measurement is in the VBY and VCY inputs. The motor bus measures the three phases (VAZ, VBZ, and VCZ). For consistency in the frequency measurement, the source voltages need to be the reference because they are strong sources and their frequency does not change drastically over time. The frequency estimation settings in the SEL-451 should reflect those in Figure 3. Single-phase measurement from Phase A is assumed. The signal XTOSRC1 (transfer to Source 1), described in detail in the "Source Selection" section, indicates that VBY will be used when XTOSRC1 = 1 and VCY is otherwise. With this arrangement, there is a solid frequency reference coming from the transfer source.

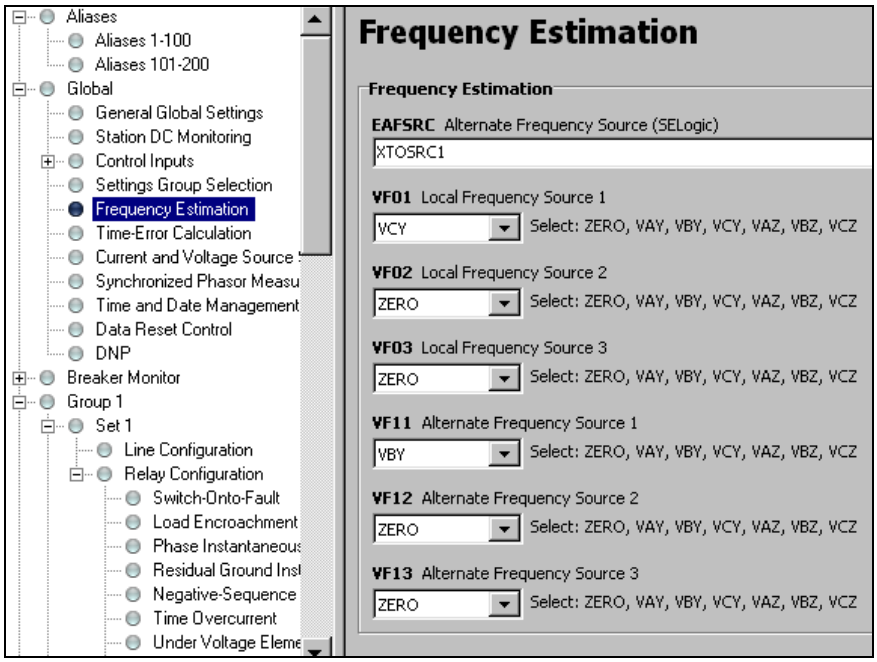

Figure 3 Frequency Estimation Settings

Source Selection

The breaker position contacts (52a) and the presence of current are used in the internal logic of the SEL-451 to derive signals 52ACL1 (Breaker 1 closed) and 52ACL2 (Breaker 2 closed). The logic shown in Figure 4 is implemented in the automation logic of the SEL-451.

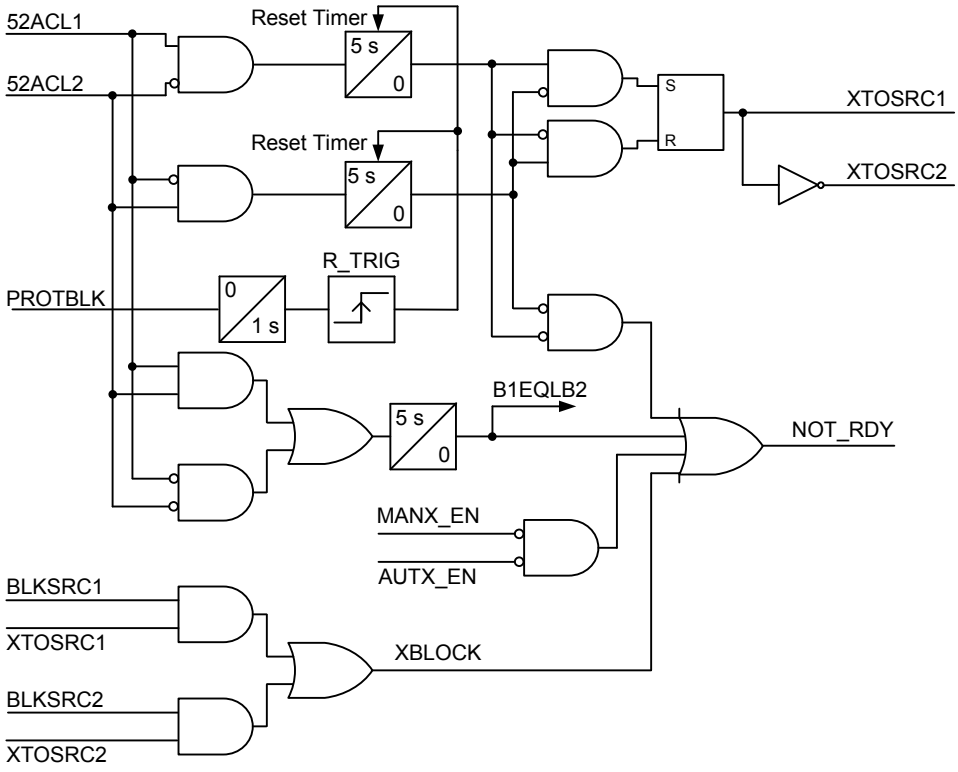

Figure 4 Transfer Source Selection Logic

The logic in Figure 4 requires that one breaker be closed and the other be opened for at least 5 seconds to identify the breaker to use in the source transfer. The setting PROTBLK (set in the protection logic) disables the transfer source selection and the whole transfer logic. The signal NOT_RDY is used in the logic of the transfer schemes to disable the logic. The settings BLKSRC1 and BLKSRC2 (set in the automation logic) block the transfer to the selected source when set to 1 (TRUE). The Relay Word bits and settings for the logic described in Figure 4 are also given in Table 1.

Table 1 Settings and Relay Word Bits for Transfer Source Selection Logic

Name	Relay Word Bit/Setting	Description
52ACL1 52ACL2	Relay Word bits	Indicates if the Source 1 or Source 2 breaker is closed by sensing the respective breaker 52a inputs (shown as IN101 and IN102 in Figure 1) and the presence of current. These Relay Word bits are derived in the internal logic of the SEL-451.
PROTBLK	Setting	Set in the protection logic. Disables the source transfer logic. It is meant for sensing trips of adjacent protective relays (the bus protective relay, for example). However, it can be used for other purposes.
BLKSRC1 BLKSRC2	Settings	Set in the automation logic. Disables the transfer to the selected transfer source.
XBLOCK	Relay Word bit	Blocks transfer.
MANX_EN	Relay Word bit	Enables manual transfer. Reflects the position of the pushbutton (PB1).
AUTX_EN	Relay Word bit	Enables automatic transfer. Reflects the position of the pushbutton (PB2).
B1EQLB2	Relay Word bit	Indicates if Breaker 1 and Breaker 2 are either both open or both closed.
NOT_RDY	Relay Word bit	Indicates that transfer logic is not ready. Reflected in target LED09.
XTOSRC1 XTOSRC2	Relay Word bits	Transfers to Source 1 or 2.

Analog Measurements

During the opening of the present source breaker, the motor bus frequency is a quantity that can drastically change in a very short period of time. In order to accurately track motor bus frequency, a measurement with a fast update is required.

The SEL-451 deterministically evaluates the protection logic every one-eighth of a power system cycle. The motor bus transfer requires that the frequency in the bus be evaluated at the same rate the SEL-451 implements the transfer logic.

The algorithm is based on measuring the angle of the Phase A voltage (VAZ input) over a period of time and comparing the difference of the measurement to the expected angle. For example, the phase angle should be exactly the same every cycle if the frequency is exactly at nominal frequency (e.g., 50 or 60 Hz). If the operating frequency is lower (less than the nominal 50 or 60 Hz), then the angle a full cycle later is not the same and the voltage angle will lag the measurement from 1 cycle ago. The change in angle is negative, implying a negative frequency difference from nominal. The measurement is used to estimate the frequency.

The angle difference can also be calculated every 0.5-cycle period using a first in, first out (FIFO) memory buffer with four memory element registers corresponding to one-half of a cycle of memory. The logic to implement this is shown in Figure 5.

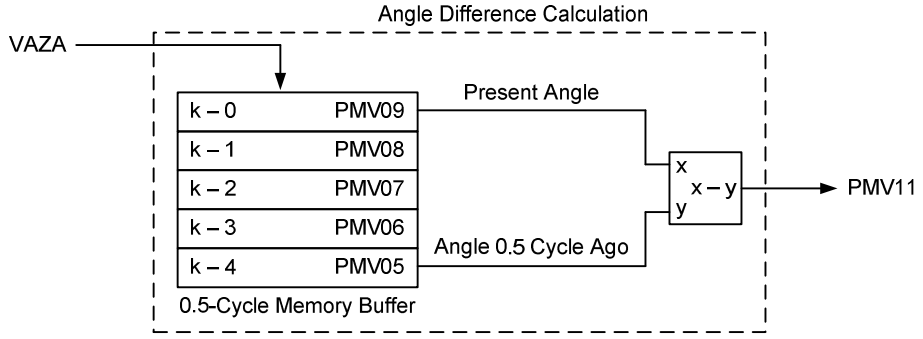

Figure 5 Memory of the Measured Angle and 0.5-Cycle Angle Difference

Whenever two angles are added or subtracted, the result can be larger than 360 degrees (for example, 180 degrees + 190 degrees = 370 degrees). In order to make sure this does not introduce problems in the algorithm, the angle difference is bounded between +180 degrees and –180 degrees.

With the angle difference ($\Delta\delta$) known, the frequency of the motor bus can be evaluated:

$$\mathrm{MBFREQ} = \mathrm{FREQ} + (\Delta\delta)\left(\frac{\mathrm{FREQ}}{180^\circ}\right) \tag{1}$$

where:

MBFREQ is the calculated motor bus frequency (PMV12).

FREQ is the calculated frequency from the frequency tracking algorithm in the SEL-451.

$\Delta\delta$ is the bounded 0.5-cycle angle difference calculated (PMV11).

Some filtering is provided to smooth out any errant angle measurements. A simple infinite impulse response (IIR) filter is used to filter the frequency. A general equation describing the filtering is given below.

$$\mathrm{MBFREQF_k} = \alpha \bullet \mathrm{MBFREQ_k} + (1-\alpha) \bullet \mathrm{MBFREQ_{k-1}} \tag{2}$$

where:

MBFREQF is the filtered motor bus frequency.

α is the filtering constant, a number between 0 and 1.

k is the present sample.

The source frequency is estimated with the same algorithm described above. For the sake of brevity, this logic is not shown in detail here, but can be viewed in the settings file that accompanies this application guide. The difference between the two frequencies measured (MBFREQF [filtered motor bus frequency] and SBFREQF [filtered source frequency]) can be calculated as the slip frequency:

$$\mathrm{SMSLIP_k} = \mathrm{SBFREQF_k} - \mathrm{MBFREQF_k} \tag{3}$$

The slip frequency is also run through an IIR filter to remove any errant measurements and ensure the calculated slip frequency is a steady, stable quantity. This filtering is similar to the IIR filtering used for the motor bus frequency and can be seen in detail in the settings file that accompanies this application guide. The change of slip is needed to calculate the compensated angle. In the logic, the change of slip is calculated over a full cycle (or 8 processing intervals):

$$DSLIPDT_k = \left(SMSLIP_k - SMSLIP_{k-8}\right) \bullet \frac{1}{\Delta t} \quad (4)$$

where:

Δt is one full period, or 8 processing intervals.

This again is because DSLIPDT is calculated over 1 cycle, or 8 processing intervals. Because the processing interval will vary as the relay tracks frequency, we can prove the following relationship:

$$\Delta t = \frac{1}{FREQ} \quad (5)$$

where:

FREQ is the calculated frequency from the frequency tracking algorithm in the SEL-451.

Similarly, DSLIPDT is run through yet another IIR filter to ensure steady, stable quantities.

Armed with the slip and the change in slip with respect to time, we can calculate the compensation angle, or the angle including the closing time of the breaker. The compensation angle is then calculated using:

$$\Delta\delta comp_k = SMSLIP_k \left(T\_BKR\right) + \frac{1}{2} \bullet DSLIPDT_k \bullet \left(T\_BKR^2\right) \quad (6)$$

where:

T_BKR is the breaker closing time in seconds.

This is a setting entered by the user in the automation logic in cycles and converted to seconds internally. Note that in the logic, there are two T_BKR1 and T_BKR2 variables to accommodate situations where the two breakers, BKR1 and BKR2, have different closing times.

IMPLEMENTING MOTOR BUS TRANSFER MODES IN THE SEL-451

The transfer scheme HMI utilizes front-panel pushbuttons to control the breakers and enter modes of operation. SEL-451 pushbutton light-emitting diodes (LEDs) are used to confirm the mode selection and the breaker status. The SEL-451 target LEDs are used for indication.

The display in the SEL-451 can be programmed to show a single-line diagram and the status of the breakers feeding the motor bus. Moreover, a customized set of display points shows important information to the user. The display points and HMI can be adjusted to meet particular user needs and use the bay control features in the SEL-451. The pushbuttons, LEDs, and liquid crystal displays (LCDs) described are simple interfaces intended for illustration purposes.

HMI, Programmable Pushbuttons, and Target LEDs

The HMI consists of a single-line diagram that is displayed on the SEL-451 LCD display. The single-line diagram illustrates the status of the controlled breakers, as shown in Figure 6. The diagram also allows the controlling of the breakers through the display using the cursor and **<Enter>** keys.

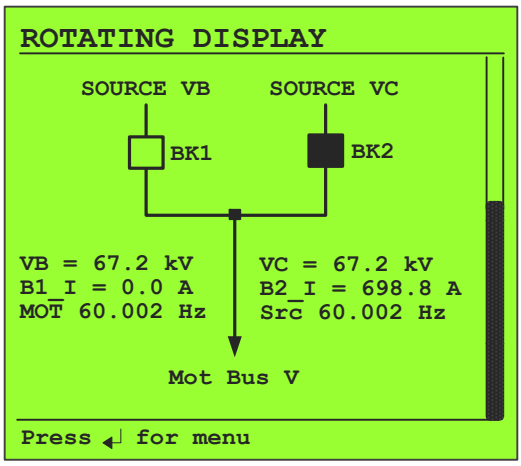

Figure 6 Single-Line Diagram

The display in Figure 6 shows the voltage and current for each source. The motor bus frequency is also displayed as well as the frequency for the source that is selected for the motor bus to be transferred to. For example, should a transfer occur, the motor bus will be transferred to Source 1. The frequency for Source 1 is displayed in the rotating display in Figure 7 as **SB Freq** at approximately 60 Hz.

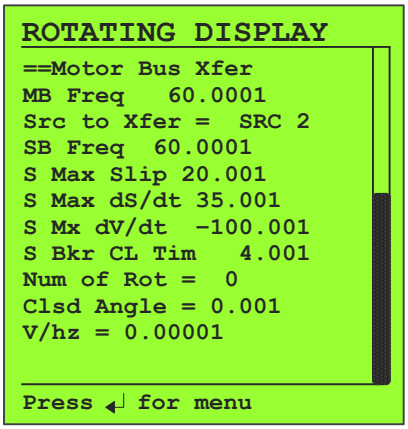

Figure 7 Important Information Shown in the Display Points

Display points in the SEL-451 are used to show important information about the transfer.

Additionally, the pushbuttons are used to perform control actions, and the pushbutton LEDs are used to provide visual indication. Figure 8 shows the pushbutton assignments for the user interface. Table 2 summarizes the functionality.

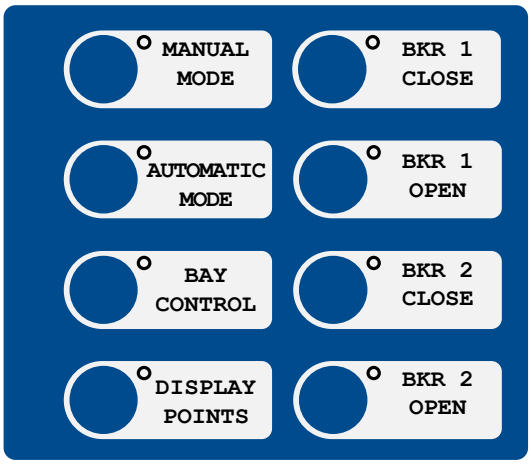

Figure 8 Pushbutton Assignments

Table 2 Description of Programmable Pushbutton Functions

Pushbutton	Label	Description
PB1	MANUAL MODE	When this mode is active, the opening or closing of a source breaker immediately starts the transfer sequence. A user in front of the SEL-451 can activate this mode. The confirmation of this mode is a blinking LED next to the pushbutton.
PB2	AUTOMATIC MODE	When automatic mode is enabled, the SEL-451 initiates the transfer when it detects the opening of a source breaker.
PB3	BAY CONTROL	Stops the LCD display rotation, and shows the single-line diagram.
PB4	DISPLAY POINTS	Stops the LCD display rotation, and shows the display points.
PB5	BKR 1 CLOSE	Controls the closing of Breaker 1. If the manual mode is active (PB1 and blinking LED), the source transfer is initiated when the pushbutton is operated.
PB6	BKR 1 OPEN	Controls the opening of Breaker 1. If the manual mode is active (PB1 and blinking LED), the source transfer is initiated when the pushbutton is operated.
PB7	BKR 2 CLOSE	Controls the closing of Breaker 2. If the manual mode is active (PB1 and blinking LED), the source transfer is initiated when the pushbutton is operated.
PB8	BKR 2 OPEN	Controls the opening of Breaker 2. If the manual mode is active (PB1 and blinking LED), the source transfer is initiated when the pushbutton is operated.

In addition to the LEDs on the programmable pushbuttons, target LEDs are also used to display information related to the motor bus transfer scheme. Table 3 summarizes the functionality of the target LEDs, and Figure 9 shows the assignments.

Table 3 Summary of Programmable Target LED Functions

Target LEDs	Label/Definition	Description
LED01	EXT XINIT_EN External initiation enabled	External event to the logic is expected to initiate the transfer logic. This external event could be a fast 52b contact changing states or a pushbutton being pressed or the contact from an upstream relay.
LED02	FASTX_EN Fast sequential transfer enabled	Sequential fast transfer mode is enabled. This LED reflects the setting EFASTTR (enable fast transfer mode) in the automation settings.
LED03	IN PHASEX_EN In-phase transfer enabled	In-phase transfer mode is enabled. This LED reflects the setting EPHSTR (enable in-phase transfer) in the automation settings.
LED04	RESIDUALX_EN Residual transfer enabled	Residual transfer mode is enabled. This LED reflects the setting ERESTR (enable residual transfer) in the automation settings.
LED05	Not used	
LED06	BLOCK XFER Transfer blocked	Conditions are programmed to block the transfer to the logically selected source.
LED07	XFER TO VBY Transfer to VBY	The source to transfer to is connected to VBY.
LED08	XFER TO VCY Transfer to VCY	The source to transfer to is connected to VCY.
LED09	LOGIC READY Transfer logic ready	The transfer logic is ready, when active. If this LED is not active, the transfer logic is not ready.
LED10	FAST OP Fast mode operated	The last transfer was during the fast transfer mode.
LED11	IN PHASE OP In-phase mode operated	The last transfer was during the in-phase mode.
LED12	RESIDUAL OP Residual mode operated	The last transfer was in the residual mode.
LED13	Not used	
LED14	VMOT ON Motor voltage on	The motor bus voltage is healthy (VMOT > 55 secondary V). This LED reflects the VAZ input.
LED15	VBY ON	The source voltage VBY is healthy (VBY > 55 secondary V).
LED16	VCY ON	The source voltage VCY is healthy (VBY > 55 secondary V).

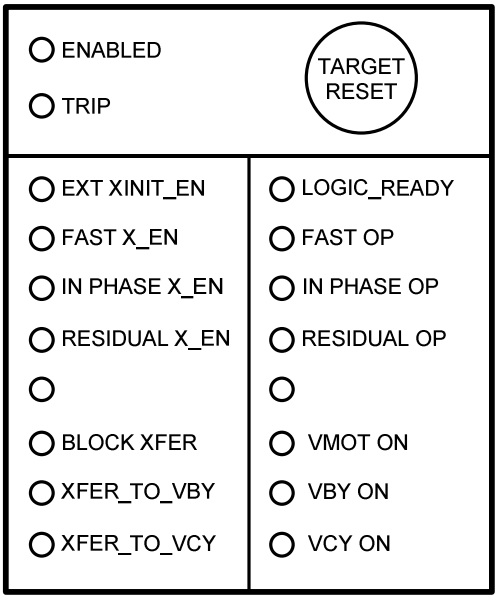

Figure 9 Assignments of Target LEDs

The HMI scheme described above illustrates a simple approach. The SEL-451 front panel is flexible to be programmed in a different way. Moreover, the bay controller functionality has not been used in this application guide; however, can provide additional functionality, such as local and remote control preferences. Please contact SEL if a different HMI scheme is required.

Modes of Operation

The scheme has provisions for two basic modes of operation: manual mode and automatic mode. The intent is to have the scheme in either mode. When the manual mode is selected, a transfer takes place when the normally closed source breaker is opened or the normally open source breaker is closed. Internally, the logic trips the closed breaker and transfers to the alternate source. A blinking LED (PB1 shown in Figure 8 and described in Table 2) denotes this mode. When the automatic mode is selected, a transfer takes place when a closed breaker opens (detected by the loss of the 52a input and the loss of current or a fast 52b).

Transfer Initiation Logic

To enter a motor bus transfer mode, the transfer needs to be initiated by an event. The SEL-451 motor transfer logic considers the following three possible transfer initiations:

- Manual mode. The transfer initiation considers the operation of the front-panel pushbuttons. The manual mode LED should be blinking to start the transfer. The operation of the **{CLOSE}** pushbutton for the transfer source breaker or the operation of the **{OPEN}** pushbutton for the present source breaker initiates the transfer when both breakers are open.
- Automatic mode. The transfer initiation considers the opening of the present source breaker. The transfer is sent when both breakers are open.
- External initiation. This is a condition defined outside the manual or automatic mode. The external initiation enable must be set to 1 (EEXTINI = 1 in the automation logic), and the external condition should be defined in the protection logic (EXTXINI).

The logic in Figure 10 implements the transfer mode initiation. The signal XFERINI starts the transfer. The Relay Word bits and settings associated with the transfer initiation logic are provided in Table 4.

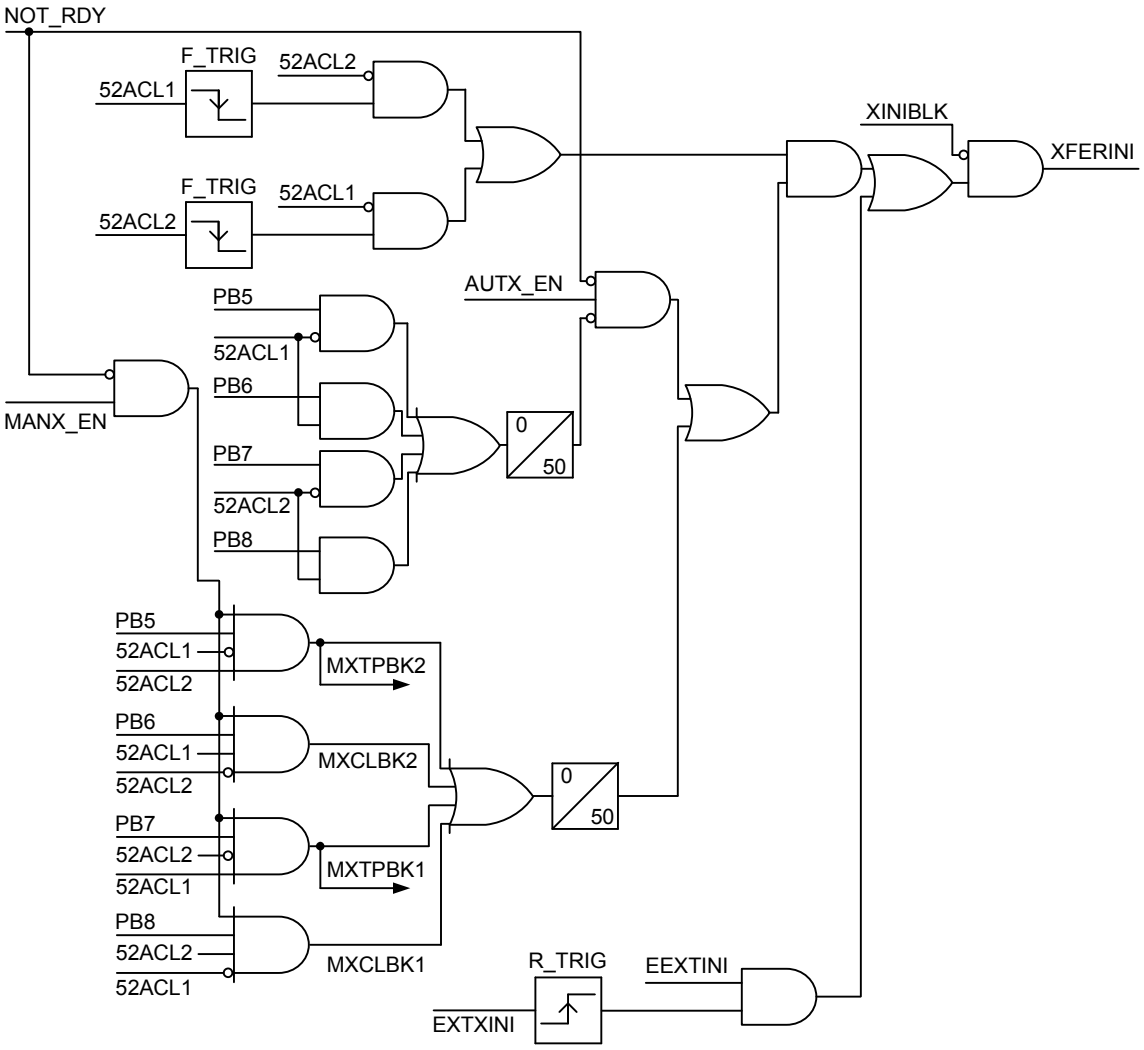

Figure 10 Transfer Initiation Logic

Table 4 Relay Word Bits and Logic Settings for Transfer Initiation Logic

Name	Relay Word Bit/Setting	Description
52ACL1 52ACL2	Relay Word bits	Indicate if the Source 1 or Source 2 breaker is closed by sensing the respective breaker 52a inputs (shown as IN101 and IN102 in Figure 1) and the presence of current. Derived in the internal logic of the SEL-451.
NOT_RDY	Relay Word bit	Denotes that the logic is not ready to proceed. Defined in Figure 4.
MANX_EN	Relay Word bit	Enables manual transfer. Reflects the position of the pushbutton (PB1).
AUTX_EN	Relay Word bit	Enables automatic transfer. Reflects the position of the pushbutton (PB2).
PB5, PB6, PB7, PB8	Relay Word bits	PB5 closes Breaker 1, PB6 opens Breaker 1, PB7 closes Breaker 2, and PB8 opens Breaker 2 (pushbutton bits).
XINIBLK	Setting	Blocks transfer initiation in the protection logic. User-defined condition.
EEXTINI	Setting	Enables external initiation in the automation logic.
EXTXINI	Setting	Enables external transfer initiation in the protection logic.
XFERINI	Relay Word bit	Indicates transfer initiation.

Transfer Mode Logic

Logically, when the SEL-451 motor bus transfer scheme enters a transfer sequence, it will be in one of either the fast, in-phase, or residual modes, depending on the selected transfer modes and system conditions. The XFERINI signal initiates the fast transfer mode, if enabled (EFASTTR = 1). If the fast transfer mode is not enabled, the in-phase transfer mode is initiated, if enabled (EPHSTR = 1). If neither the fast nor the in-phase mode is enabled, the residual mode is initiated, if enabled (ERESTR =1).

Once in a particular mode, the logic implements the required checks to issue the close signal within the time window allocated to the mode. Once the fast transfer mode terminates its allocated time, the in-phase mode is enabled. Once the in-phase mode finishes its allocated time, the residual mode is entered.

If any of the modes send a close command, the logic resets. The SEL-451 requires the signal NOT_RDY = 0 and a new XFERINI to start a new transfer again. The assertion of PROTBLK disables all the modes and requires a new XFERINI for a new transfer.

The logic governing the transfer modes is shown in a logic diagram in Figure 11. In addition, the Relay Word bits and logic settings associated with the three transfer modes are summarized in Table 5.

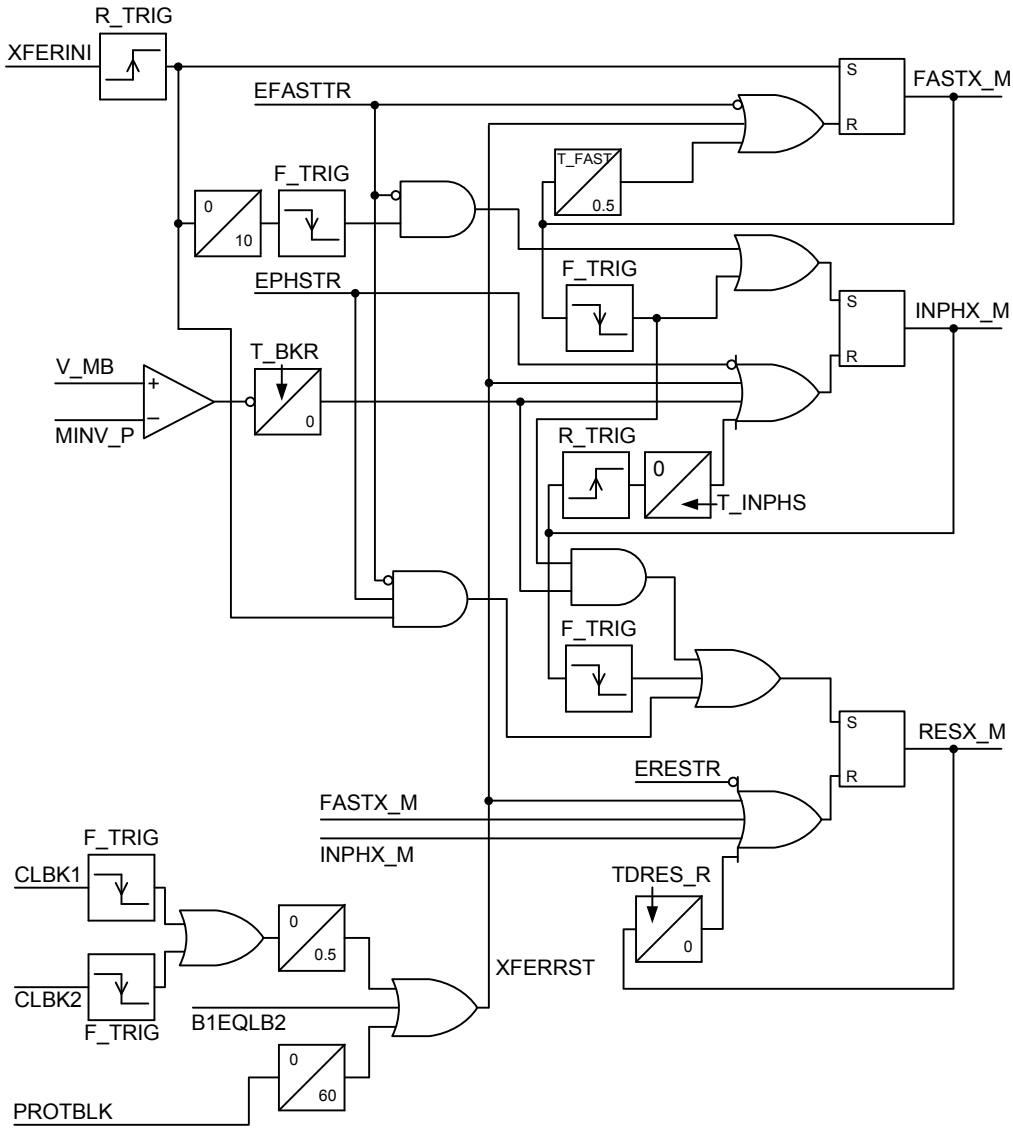

Figure 11 Transfer Mode Logic

Table 5 Relay Word Bits and Logic Settings for Transfer Mode Logic

Name	Relay Word Bit/Setting	Description
XFERINI	Relay Word bit	Indicates transfer initiation.
EFASTTR	Setting	Enables fast transfer mode in the automation logic.
EPHSTR	Setting	Enables in-phase transfer in the automation logic.
ERESTR	Setting	Enables residual transfer in the automation logic.
CLBK1 CLBK2	Relay Word bits	Close Breaker 1 and Breaker 2. Signals are from the motor bus transfer logic.
PROTBLK	Setting	Set in the protection logic. Disables the source transfer logic. It is meant for sensing trips of adjacent protective relays (the bus protection relay, for example). However, it can be used for other purposes.
B1EQLB2	Relay Word bit	Indicates that Breaker 1 and Breaker 2 are either both open or both closed.
XFERRST	Relay Word bit	Clears the logical modes.
FASTX_M	Relay Word bit	Activates fast transfer mode.
INPHX_M	Relay Word bit	Activates in-phase transfer mode.
RESX_M	Relay Word bit	Activates residual transfer mode.

Fast Transfer Mode

A sequential fast transfer takes place in the first few cycles after the present source breaker is opened. A simultaneous transfer occurs when the trip command of the closed breaker is sent simultaneously with the close command of the open breaker. The ESIMFX input to the logic in Figure 12 is used to identify a simultaneous transfer mode. A sequential fast transfer verifies the opening of the closed breaker and issues the close signal. This is shown by the 52ACL1 and 52ACL2 logic applied to the AND gate at the bottom of Figure 12.

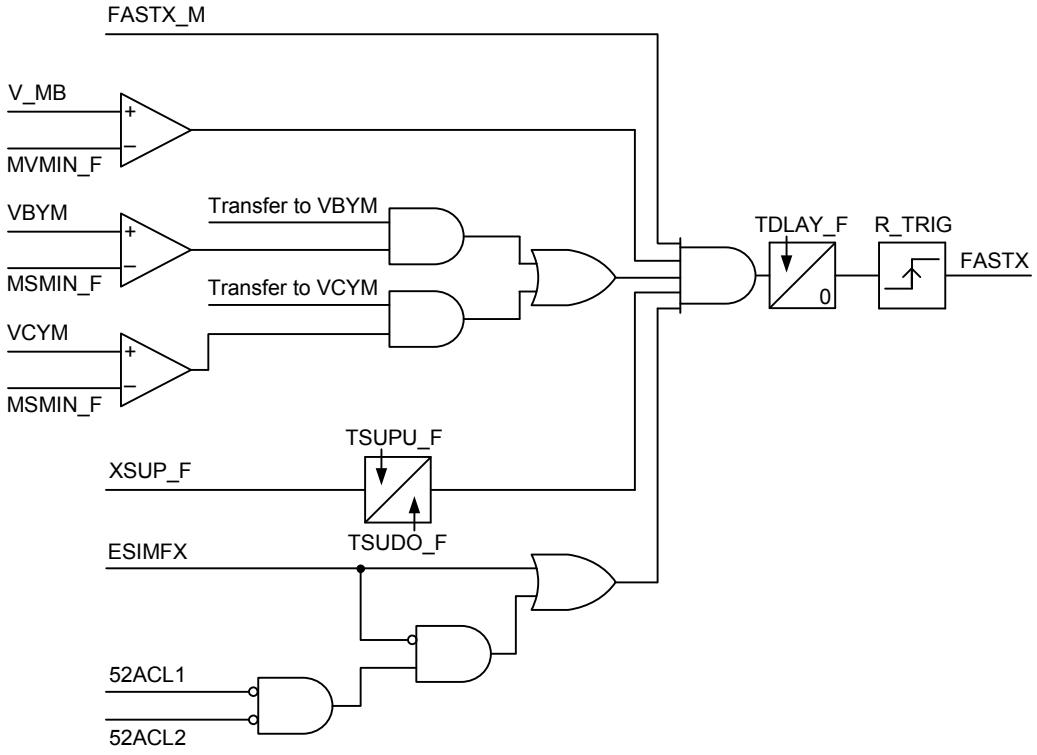

Figure 12 Fast Transfer Mode Logic

The Relay Word bits and settings associated with the fast transfer mode are summarized in Table 6 and Table 7, respectively.

Table 6 Relay Word Bits and Logic Settings for Fast Transfer Mode

Name	Relay Word Bit/Setting	Description
FASTX_M	Relay Word bit	Activates fast transfer mode.
52ACL1 52ACL2	Relay Word bits	Indicate if the Source 1 or Source 2 breaker is closed by sensing the respective breaker 52a inputs (shown as IN101 and IN102 in Figure 1) and the presence of current. These Relay Word bits are derived in the internal logic of the SEL-451.
FASTX	Relay Word bit	Denotes the operation of the fast transfer mode.
XSUP_F	Setting	Set in the protection logic. Condition to supervise the fast transfer. A synchronism-check element would normally be used here for supervision.

Table 7 Fast Transfer Mode Settings

Name	Range	Description
EFASTTR	1 := ENABLED 0 := DISABLED	Fast transfer mode.
ESIMFX	1 := ENABLED 0 := DISABLED	Simultaneous fast transfer mode. If enabled, the close signal to the open breaker is sent simultaneously with the open signal to the closed breaker.
T_FAST	Number of cycles	Time duration of the fast transfer mode.
SVMIN_F	Secondary V	Minimum source voltage for the fast transfer mode to operate.
MVMIN_F	Secondary V	Minimum motor bus voltage for the fast transfer mode to operate.
TDLAY_F	Number of cycles	Close command delay.
MXSLP_F	Hz	Maximum slip for the fast transfer mode to operate.
TSUPU_F	Number of cycles	Supervision condition pickup.
TSUDO_F	Number of cycles	Supervision condition dropout.

In-Phase Transfer Mode

The in-phase transfer mode issues the close signal, assuming the rate of change of slip and the operating time of the breaker, in order to obtain a close to zero angle difference when the breaker contacts close. The nonlinearities of the load torque, the motor flux decay, and the logic processing interval of the SEL-451 make it a challenge to obtain perfect results. The in-phase transfer mode tries to minimize the angle difference between the motor bus voltage (VAZ) and the active transfer source voltage (VBY or VCY) when the breaker contacts actually close. The logic associated with the in-phase transfer mode is shown in Figure 13. The Relay Word bits and settings are summarized in Table 8 and Table 9, respectively.

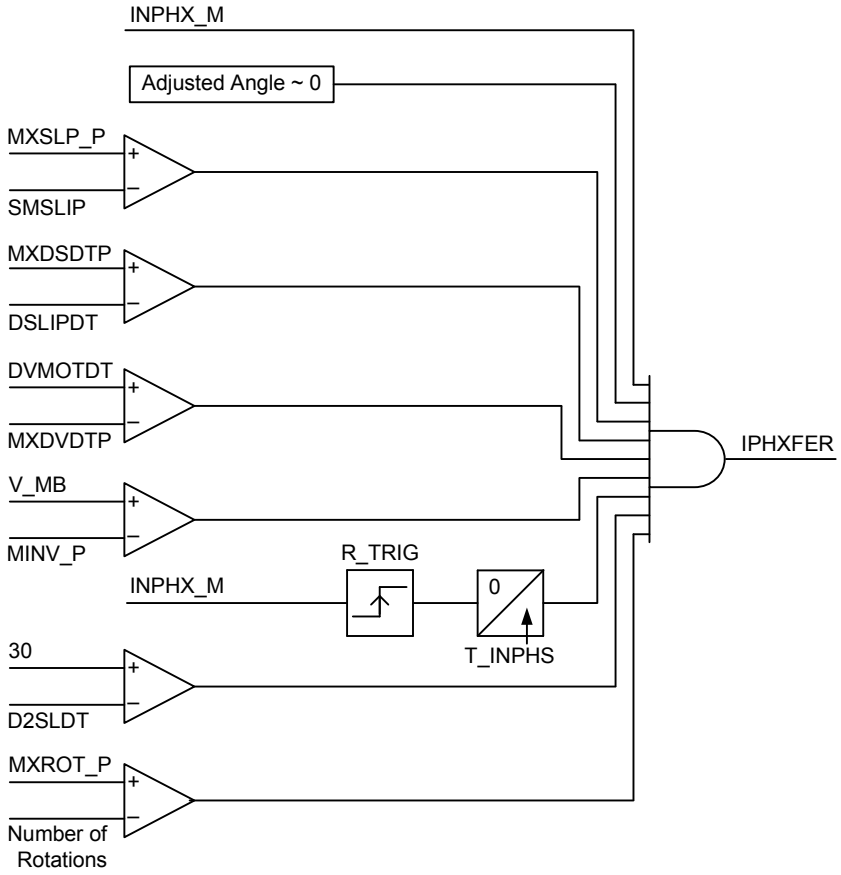

Figure 13 In-Phase Transfer Mode Logic

Table 8 Relay Word Bits for In-Phase Transfer Mode

Name	Relay Word Bit/Setting	Description
INPHX_M	Relay Word bit	Activates in-phase transfer mode.
IPHXFER	Relay Word bit	Denotes the operation of the in-phase transfer mode.

Table 9 In-Phase Transfer Mode Settings

Name	Range	Description
EPHSTR	1 := ENABLED 0 := DISABLED	In-phase transfer mode.
MXSLP_P	Hz	Maximum slip allowed before issuing the close command.
MXDSDTP	Hz/second	Maximum rate of change of slip before issuing the close command.
MXDVDTP	Secondary V/second	Maximum rate of voltage decay (secondary V/second) before issuing the close command.
MINV_P	Secondary V	Minimum motor bus voltage magnitude before issuing the close command.
T_INPHS	Number of cycles	Total time window for the in-phase transfer.
MXROT_P	Number of rotations	Maximum number of rotations allowed in the in-phase transfer mode.

During the development and testing of the scheme, we noticed that a zero-degree angle closing is practically not possible due to the nonlinearities of the load and motor dynamics. Within limits, testing has shown that closing angles are within ±30 degrees. The limits are related to the change of slip (frequency difference) over time and the closing time of the breaker. Table 10 relates the maximum permissible change in slip with respect to the closing time of the breaker.

Table 10 Breaker Closing Time and Maximum Slip Change (MXDSDTP) Setting

Breaker Closing Time in Cycles	Maximum MXDSDTP (Hz/Second)
3	40
4	35
5	30
6	25
7	20
8	15
9	10
10	5

While the rate of decay of the motor bus voltage does vary, the MXDVDTP setting in the relay does not warrant the thorough review that the rate of change of slip does. Recall that the motor bus voltage will decay and the rate of its decay is related to the load on the motor bus as well as the machine parameters of the motors on the motor bus. The parameter MXDVDTP should not be set less than –100 V/second, and as a recommended value, it should be –80 V/second.

Residual Transfer Mode

In residual transfer mode, there is a single check and a delay to add security. The mode assumes that the load is still rotating and the motor bus voltage has decayed sufficiently to close the transfer source breaker, ensuring no damage to the connected machines. The logic for the residual transfer is shown in Figure 14.

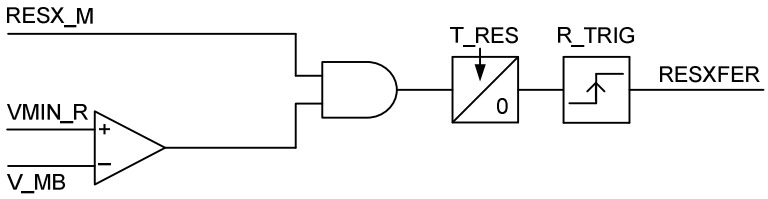

Figure 14 Residual Transfer Mode Logic

The RESX_M bit activates the residual transfer mode. This bit is described in Figure 11. The measured motor bus voltage magnitude, denoted as V_MB in Figure 14, is compared to the setting VMIN_R. If the measured voltage is less than the setting and the transfer is activated (RESX_M is asserted), then we start a timer. The timer has a pickup setting of T_RES. The purpose of this timer is to add security and ensure the voltage is depressed because of the loss of a source. The RESXFER bit is the output of the timer through a rising edge trigger. A listing of the Relay Word bits associated with the residual transfer mode is given in Table 11, and a listing of the residual transfer mode settings is given in Table 12.

Table 11 Residual Transfer Mode Relay Word Bits

Name	Relay Word Bit/Setting	Description
RESX_M	Relay Word bit	Activates residual transfer mode.
RESXFER	Relay Word bit	Denotes the operation of the residual transfer mode.

Table 12 Residual Transfer Mode Settings

Name	Range	Description
ERESTR	1 := ENABLED 0 := DISABLED	Residual transfer mode.
VMIN_R	Secondary V	Maximum motor bus voltage to enable the transfer.
T_RES	Number of cycles	Time delay after reaching the maximum motor bus voltage.

USE OF INTERNAL SEL-451 LOGIC

The core of the logic for the scheme is implemented in SELOGIC control equations. Parts of the SEL-451 firmware logic are also used to provide a complete scheme.

Manual trip logic, manual close logic, and synchronism-check logic are used to complement the motor bus transfer logic programmed in the protection and automation logic.

Several protection functions are still available for bus protection or backup protection. These include definite time, instantaneous and inverse overcurrent (50/51), undervoltage and overvoltage (27/59), frequency (81), and demand elements. The application of these elements is out of the scope of this application guide. The elements should be programmed to trip in the manual trip equation, as described in the "SEL-451 Breaker Trip Equations" section of this application guide.

SEL-451 Breaker Close Equations

The SEL-451 logic and settings include provisions for automatic reclosing and manual closing. The reclosing logic should be turned off (E79 := N), but the manual closing equations are used. The settings associated with reclosing and manual closing are shown in Figure 15 and summarized in Table 13.

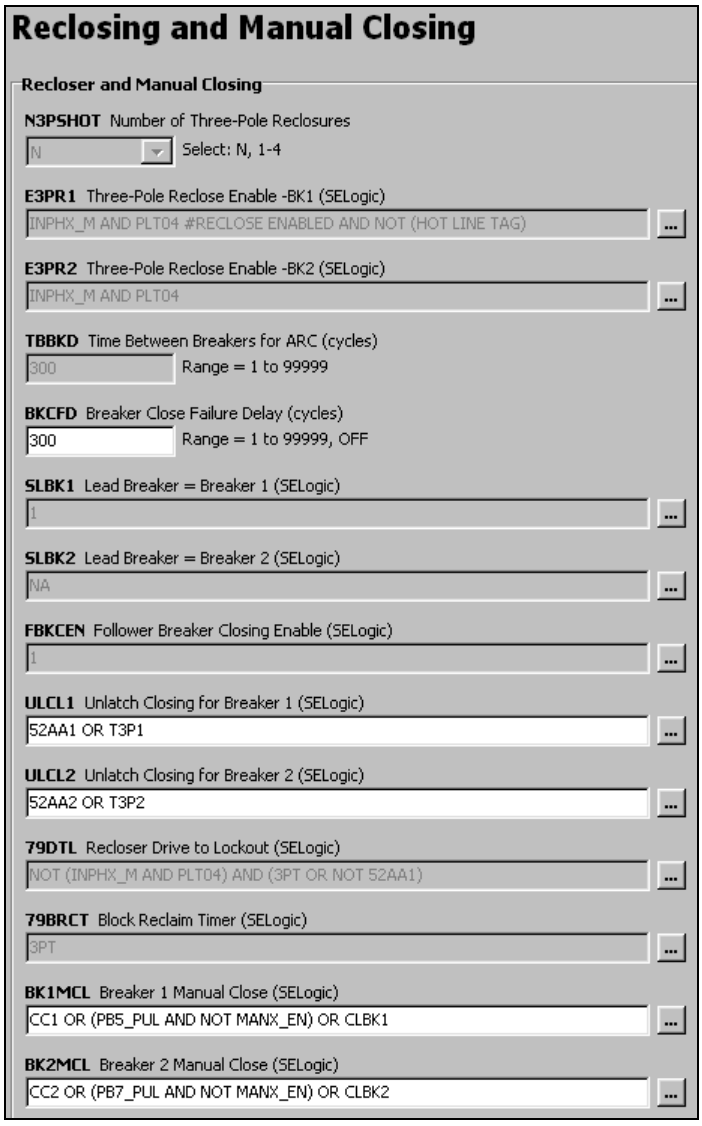

Figure 15 Reclosing and Manual Closing Settings in the SEL-451

Table 13 Applicable Settings in the Reclosing and Manual Closing Settings

Name	Description
BKCFD	Time used to denote the failure of the breaker to close after the close command has been issued. When the logic operates, Relay Word bit BK1CFT or BK2CFT asserts.
ULCL1 ULCL2	Conditions to unlatch the close signal. Normally, the 52a input contacts or any protective or manual trip is used to unlatch the close signal.
BK1MCL BK2MCL	Conditions for manual close. CC*x* is the close command from the serial port. PB5_PUL AND NOT MANX_EN corresponds to the close pushbutton for Breaker 1, which should be active if the scheme is not in the manual transfer mode. PB7_PUL is similar, but for Breaker 2. CLBK1 and CLBK2 are the transfer logic close commands.

The close failure logic in the SEL-451 asserts bit BK1CFT (or BK2CFT) if the close command has been sent (BK1CL or BK2CL) and the breaker status indicates that the breaker is still open. The bits should be used in disabling the transfer logic (protection logic PROTBLK).

SEL-451 Breaker Trip Equations

The trip logic in the SEL-451 should be bypassed for this application to control the opening of the breakers individually. The trip equation (TR) can contain elements that would send the trip command to both breakers. The manual trip equations should be used to define the opening conditions of the breakers, as shown in Figure 16. Additionally, the settings are summarized in Table 14.

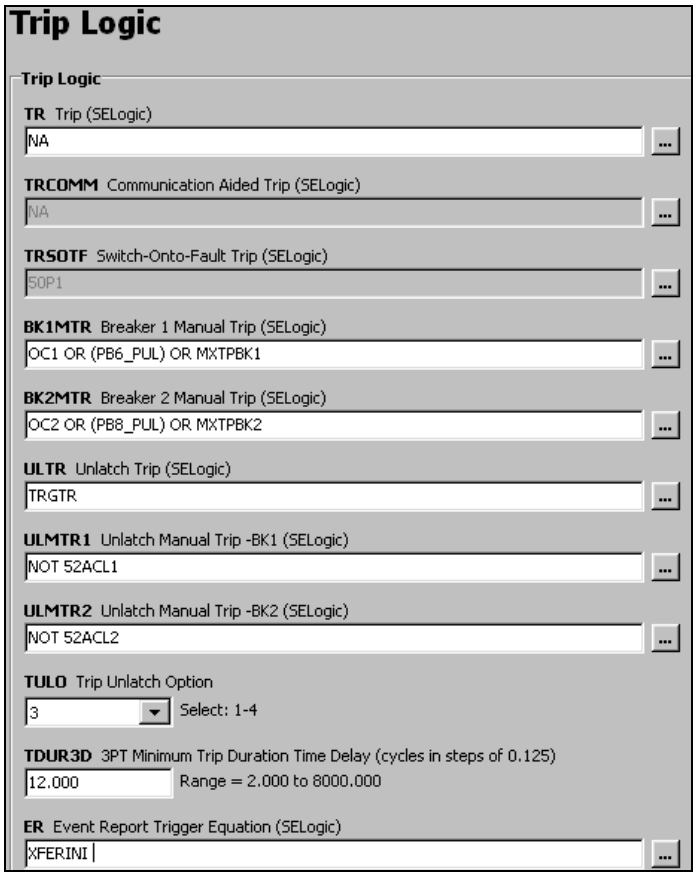

Figure 16 Trip Logic Settings in the SEL-451

Table 14 Applicable Settings in the Trip Logic Settings

Name	Description
TR	Trip equation common to both breakers. Preferably, it should be left out unless the trip is sent to both breakers.
BK1MTR BK2MTR	Manual trip conditions for Breakers 1 and 2. These equations should be used to identify opening conditions going to each breaker. In Figure 16, OC*x* is the communications breaker opening, PB6 is the open pushbutton for Breaker 1, and PB8 is the open pushbutton for Breaker 2. MXTPBK1 (manual transfer, trip Breaker 1) is used to send the open signal for a manual transfer for Breaker 1. MXTPBK2 is the signal for Breaker 2.
TDUR3D	Minimum trip signal duration. Ensures that the output contacts will be closed for at least the TDUR3D setting, which is given in cycles.
ER	Event report trigger. Starts the capture of an event report. XFERINI makes the SEL-451 capture an event when a transfer is started.

SEL-451 Synchronism Check

Although the synchronism-check function in the SEL-451 is too slow for the actual motor bus transfer scheme, it can be used to qualify the fast bus transfer. XSUP_F (in the protection logic) is the place where the supervision should be placed. For a complete description of the synchronism-check element and settings, refer to the SEL-451 instruction manual (available at http://www.selinc.com). Pertinent settings are summarized in Table 15 and shown in Figure 17.

Table 15 Applicable Synchronism-Check Settings

Name	Description
SYNCP	Synchronism-check reference. It should be the VAZ voltage.
25VH 25VL	High and low thresholds for a healthy reference voltage.
SYNCS1 SYNCS2	Synchronizing voltage. For Source 1, it should be VBY. For Source 2, it should be VCY.
KS*x*M KS*x*A 25SFBK*x* ANG1BK*x* ANG2BK*x*	Synchronism-check settings described in the SEL-451 instruction manual. ANG1BK*x* is the first angle threshold for the synchronism-check function.
BSYNBK*x*	Synchronism-check block for Breaker *x* (*x* = 1 or 2). The algorithm can be blocked if the transfer scheme is not ready (NOT_RDY), the breaker is closed (52ACL1 or 52ACL2), or the transfer is to the other breaker (XTORC2 for Breaker 1).

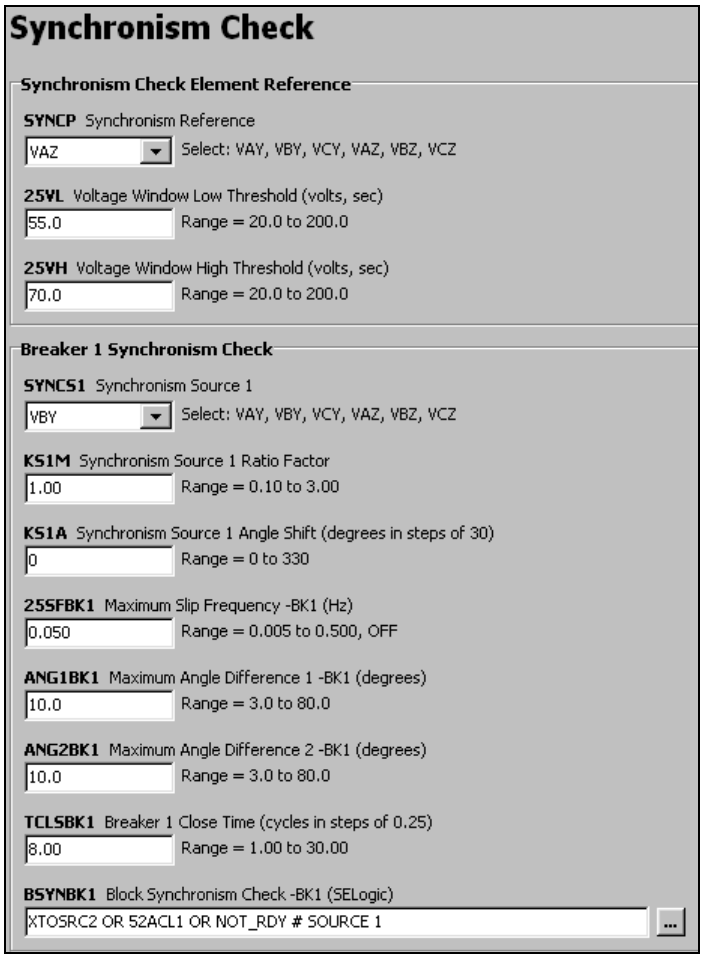

Figure 17 Synchronism-Check Settings in the SEL-451

SEL-451 Breaker Failure

The SEL-451 provides breaker failure for both controlled breakers. Recall that breaker failure is strongly recommended when simultaneous fast transfer is applied. It requires the presence of current in the IW and IX inputs. Refer to the SEL-451 instruction manual for a complete description of breaker failure logic. The pertinent settings are provided for convenience in Table 16.

Table 16 Applicable Breaker Failure Settings

Name	Description
50FP1 50FP2	Breaker failure overcurrent pickup for Breaker 1 and Breaker 2.
BFPU1 BFPU2	Breaker failure time delay for Breaker 1 and Breaker 2.
BFI3P1 BFI3P2	Breaker failure initiation for Breaker 1 and Breaker 2.

APPLICATION EXAMPLE

The customized SELOGIC control equations for motor bus transfer implemented in the SEL-451 are flexible enough to accommodate different application requirements. The purpose of this application example is to illustrate the possible configuration capabilities of the SEL-451 scheme, which does not imply this example is the only application solution that will work. It is important to remember that the knowledge of the motor bus dynamic behavior and the attached mechanical loads to the motors is important. Dynamic studies and/or rundown tests can provide the information to assess the feasibility of the transfer and the transfer modes to be used. The SEL-451 performs the transfer modes if the measurements are within its settings and refrains from issuing the close command if not. Decay rates of both frequency and voltage magnitude are different depending on the number of motors on the motor bus, the loading of each, and the type of load.

Consider, for example, the single-line diagram in Figure 18. The motor bus containing motors M1 through M4 operates with its main feed coming from Breaker 1. The bus-tie breaker, BKR 2, is used in the transfer from the main source, Source 1 (SRC 1), to Source 2 (SRC 2) under certain conditions. Transfer from Source 2 to Source 1 is allowed under all conditions. If the transfer enters the residual transfer mode, two motors need to be disconnected from the bus (M3 and M4).

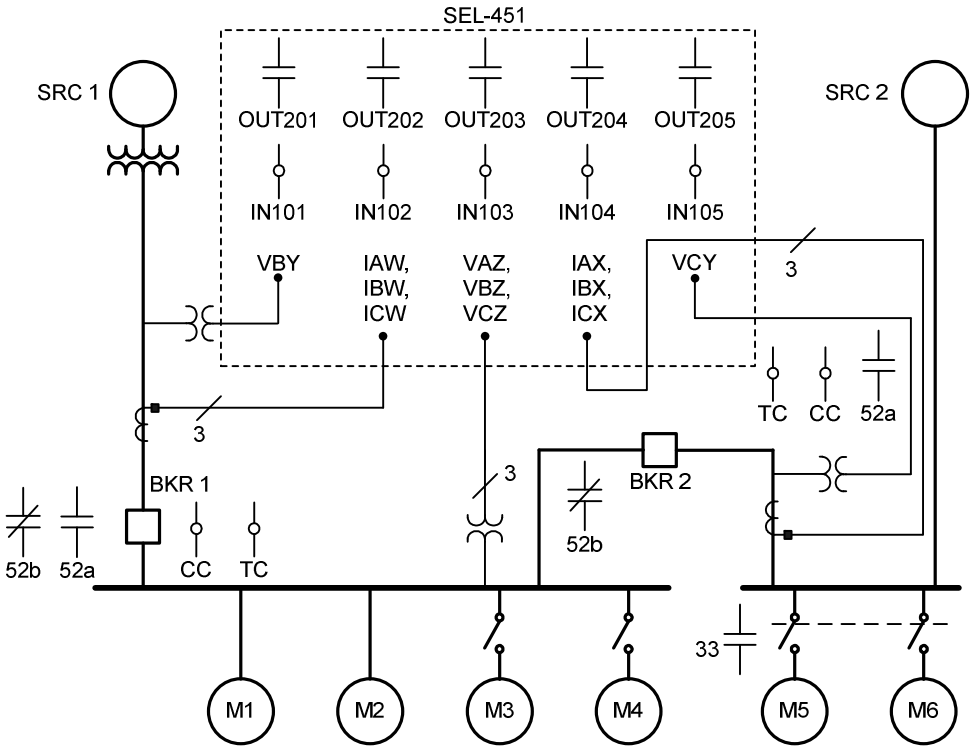

Figure 18 Application Example

Wiring

Figure 18 shows the simplified wiring. Each breaker provides a 52a (normally open breaker status) and a fast 52b (normally closed fast breaker status) to be used to implement a simultaneous fast transfer.

Two outputs are assigned for each breaker to open (trip) or close. A single output is planned to disconnect the M3 and M4 motors when the transfer enters the residual transfer mode.

Table 17 reflects the planned wiring for the SEL-451.

Table 17 Application Example Wiring for the SEL-451

Terminals	Description
I*x*W	Breaker 1 input currents (IAW, IBW, and ICW).
I*x*X	Breaker 2 input currents (IAX, IBX, and ICX).
VBY	Transfer source voltage for Breaker 1 (SRC1).
VCY	Transfer source voltage for Breaker 2 (SRC2).
V*x*Z	Motor bus voltages (VAZ, VBZ, and VCZ).
IN101	52a normally open breaker position contact for Breaker 1.
IN102	52b fast normally closed breaker position contact for Breaker 1.
IN103	33 status of the connected motors M5 and M6 (1 = closed, 0 = open).
IN104	52a normally open breaker position contact for Breaker 2.
IN105	52b fast normally closed breaker position contact for Breaker 2.
OUT201	Trip output contact for Breaker 1.
OUT202	Close output contact for Breaker 1.
OUT203	Output signaling the need to open M3 and M4.
OUT204	Trip output contact for Breaker 2.
OUT205	Close output contact for Breaker 2.

Operation Constraints

Source 1 is the utility feed and can be considered a very strong source. Source 2 can be in phase or 30 degrees out of phase with respect to Source 1. Different upstream paths to the utility feed or an alternate source introduce the phase displacement.

Because of the mechanical loads connected to M5 and M6, if either of these motors is connected to its bus, there cannot be a source transfer to Source 2. The contact (33) logically denotes that at least one motor is connected to the bus, as shown in Figure 18.

Simultaneous fast transfer can be started by a transfer to either source. Fast 52b contacts should start the transfer, and synchronism check across the breakers should supervise the transfer.

A rundown of a typical load configuration was performed. The oscillography showed that the slip frequency before it reached the residual transfer mode could be estimated at 20 Hz. The rate of decay of the slip frequency reached 20 Hz/second. The voltage magnitude decayed at around –40 V/second. The slip frequency, rate of change of slip frequency, and rate of voltage magnitude decay parameters just described are to be considered for the in-phase transfer mode.

The residual transfer mode is enabled once the motor bus voltage drops to 20 percent of nominal.

The breaker closing times are 3 cycles for each breaker. Breaker failure is used to disable any transfer in progress and is started by the fast 52b breaker position contacts.

Fast Transfer Mode Setup

The fast transfer mode is simultaneous and initiated externally by a fast 52b contact. Two inputs (IN102 for Breaker 1 and IN105 for Breaker 2) are assigned to these signals. The settings required to enable and set up fast transfer for this application example are detailed in Table 18.

Table 18 Sequential Fast Transfer Mode Settings

Name	Value	Description
EFASTTR	1	Fast transfer mode enable.
ESIMFX	1	Simultaneous fast transfer mode enable. If enabled, the close signal to the open breaker is sent simultaneously with the open signal to the closed breaker.
T_FAST	6	6-cycle fast transfer mode duration. With 3-cycle breakers, this should allow sufficient time for one breaker to close as the other is opening.
SVMIN_F	62	90 percent nominal, or 62 secondary V.
MVMIN_F	62	90 percent nominal, or 62 secondary V.
TDLAY_F	0.50	Close command delay in cycles.
MXSLP_F	10	Maximum slip frequency for the fast transfer mode to operate, in Hz.
TSUPU_F	1	Supervision condition pickup.
TSUDO_F	6	Supervision condition dropout.
XSUP_F	(XTOSRC1 AND 25A1BK1) OR (XTOSRC2 AND 25A1BK2)	Condition to supervise the fast transfer in the protection logic. A synchronism-check element would normally be used here for supervision.

The EFASTTR setting must be set to 1 to enable the fast transfer mode. ESIMFX is set to 1 because in our specific application example, simultaneous fast transfer is desired. T_FAST sets the duration of the fast transfer mode. For 3-cycle breakers, setting this to 6 cycles allows adequate time for the alternate source breaker to open as the primary source breaker opens. The transfer voltage initiation level is set at 90 percent of the nominal voltage for both the motor bus, MVMIN_F, and the source bus, SVMIN_F. This means if the voltage on either the source bus or motor bus is below 90 percent of the nominal value, a fast transfer will not occur. The idea is that the voltage magnitude has already been depressed too far for a fast transfer and one of the other transfer modes (in-phase or residual) may be more appropriate. The TDLAY_F setting, or close time delay, is set at 0.5 cycles. The maximum slip for the fast transfer mode, or MXSLP_F, is set at 10 Hz. This setting ensures that the motor bus voltage and alternate source voltage are not slipping too quickly. Closing for a slip rate higher than 10 Hz for this system risks the phase angle being too large at the time the breaker actually closes for a fast transfer. Recall that the fast transfer does not attempt to predict the phase angle and close in at zero degrees, but rather executes the transfer quickly, if possible, so that the phase angle and resultant V/Hz do not become too large. XSUP_F provides supervisory conditions for a fast transfer to occur. In this example, we include the two synchronism-check elements. So, for the case where we are transferring to Source 1, the XTOSRC1 bit is asserted and the 25A1BK1 synchronism-check element will verify that there is no standing angle difference between Source 1 and the motor bus prior to a transfer. Similarly, when we transfer to Source 2, the XTOSRC2 bit is asserted and the 25A1BK2 synchronism-check element will verify no standing angle exists.

Because the synchronism-check elements are used in the fast transfer supervision logic, the settings for the synchronism-check element for the application example are outlined in Table 19. Recall that this synchronism-check element is used to check that the phase angle between the motor bus and the alternate source is very close prior to any transfer. This is intended to check that there are no standing voltage angle differences between the two sources.

Table 19 Synchronism-Check Settings

Name	Value	Description
SYNCP	VAZ	Voltage reference set to VAZ, the Phase A voltage of the motor bus.
25VL 25VH	55.0 70.0	Low and high thresholds, in secondary V.
SYNCS1 KS1M KS1A	VBY 1.0 0.0	VBY is the Source 1 voltage to compare against VAZ.
ANG1BK1	10	Angle check set to 10 degrees.
BSYNBK1	XTOSRC2 OR 52ACL1 OR NOT_RDY	No need to evaluate this function if the transfer is to the other breaker, Breaker 1 is closed, or the logic is not ready.
SYNCS2 KS2M KS2A	VCY 1.0 0.0	VCY is the Source 2 voltage to compare against VAZ.
ANG1BK2	10	Angle check set to 10 degrees.
BSYNBK2	XTOSRC1 OR 52ACL2 OR NOT_RDY	No need to evaluate this function if the transfer is to the other breaker, Breaker 1 is closed, or the logic is not ready.

In-Phase Transfer Mode Setup

The in-phase transfer mode is the most complicated mode to implement. Creating settings for in-phase transfer requires more careful consideration than the fast or the residual transfer modes. The motor bus voltage decays and the phase angle between the source and the motor bus voltages changes over time. The goal is to close the breaker when the phase between these two voltages is zero and the magnitude of the voltage is within reasonable margins. The algorithm of the SEL-451 tries to calculate the proper time to send the close command such that the closing angle is zero when the breaker contacts have actually closed. Due to the nonlinear behavior of the load, motor dynamics, and the discrete calculation (every one-eighth of a power system cycle), closing at exactly zero degrees is extremely unlikely. The actual closing angle will deviate from, but will be close to, the target angle of zero degrees. During the testing of the scheme in a simulation mode, with the limits shown in Table 20, the closing angle should be within ±30 degrees.

If a dynamic study or rundown event(s) are available, the in-phase transfer mode parameters can be more properly applied. However, conservative estimates can also be used to initially set the mode and evaluate the initial parameters. The logic in the SEL-451 for in-phase transfer will restrain from sending the close command if the thresholds are not met and will enter the residual transfer mode.

In this application example, data from a rundown event (described previously in the "Operation Constraints" section of this application guide) are used to evaluate how to set the parameters for in-phase transfer.

Table 20 In-Phase Transfer Mode Settings

Name	Value	Description
EPHSTR	1	In-phase transfer mode enable.
MXSLP_P	30	Maximum slip. The rundown test showed that before reaching the residual levels, the slip frequency reached 20 Hz. The maximum slip may be larger in practice, so additional margin was applied. We considered that 30 Hz was a safe margin.
MXDSDTP	40	Maximum change of slip depending on the breaker closing time (suggestions defined in Table 10). In this example, the breaker closing time is 3 cycles.
MXDVDTP	–60	The rate of decay of the motor bus voltage, seen to be –40 V/second in the rundown test. Additional margin is possible to allow the transfer.
MINV_P	28	40 percent nominal.
T_INPHS	30	Total time window for the in-phase transfer in cycles.
MXROT_P	3	Three 360-degree rotations allowed during the in-phase transfer mode, or three slip cycles allowed for the in-phase transfer. After the third slip cycle, an in-phase transfer will be blocked.

Residual Transfer Mode Setup

The residual transfer mode is entered once the in-phase transfer mode is not successful or is disabled. A voltage threshold (VMIN_R) enables the close command. Table 21 shows the applicable settings for the residual voltage transfer mode in this application example. The ERESTR setting must be set to 1 to enable residual transfer. TDRES_R, or length of the residual transfer mode in cycles, is set at 120 cycles. A setting of 120 cycles allows ample time for the voltage to decay below the limit in this example system. The VMIN_R setting of 14 V, or 20 percent of nominal voltage, is discussed in the "Operation Constraints" section of this application guide. Finally, a time-delay setting, or T_RES, of 1 cycle is utilized.

Table 21 Residual Transfer Mode Settings

Name	Value	Description
ERESTR	1	Residual transfer mode enable.
TDRES_R	120	Residual transfer mode time duration, in cycles.
VMIN_R	14	20 percent nominal.
T_RES	1	Time delay after reaching the maximum motor bus voltage.

Logic and Interlocks

Logic and interlocks to initiate transfer, block transfer to Source 1 or Source 2, and to block transfers altogether are described in Table 22.

Table 22 Interlocks

Name	Value	Description
EEXTINI	1	External transfer initiation enable.
EXTXINI	(IN102 AND NOT 52ACL1) OR (IN104 AND NOT 52ACL2)	Fast 52b contacts.
BLKSRC1	0	No block for the transfer to Source 1.
BLKSRC2	IN103	M5 and M6 out-of-service block for the transfer to Source 2.
XSUP_F	(XTOSRC1 AND 25A1BK1) OR (XTOSRC2 AND 25A1BK2)	Synchronism-check supervision.
PROTBLK	(BFTRIP1 OR BFTRIP2) OR (BK1CFT OR BK2CFT)	Equation to block the transfer logic for certain conditions. The conditions to recognize are breaker failure and close failure. Other external conditions may apply, such as the trip of the bus differential relay.

Trip Logic

The SEL-451 internal trip logic settings are provided in Table 23. The trip logic can be programmed as shown in Figure 19.

Table 23 Summary of Trip Logic Settings

Name	Value	Description
TR	NA	Not used.
BK1MTR	OC1 OR (PB6_PUL) OR MXTPBK1 OR BFTR1	Manually trips the breaker when the open command is issued for Breaker 1, when PB6 (PB6_PUL) is pressed, when the manual transfer logic calls for a trip, or if a breaker failure on Breaker 1 occurs.
BK2MTR	OC2 OR (PB8_PUL) OR MXTPBK2 OR BFTR2	Manually trips the breaker when the open command is issued for Breaker 2, when PB8 (PB8_PUL) is pressed, when the manual transfer logic calls for a trip, or if a breaker failure on Breaker 2 occurs.
ULMTR1	NOT 52ACL1	
ULMTR2	NOT 52ACL2	
ER	XFERINI	Triggers an oscillographic event with a transfer initiation.

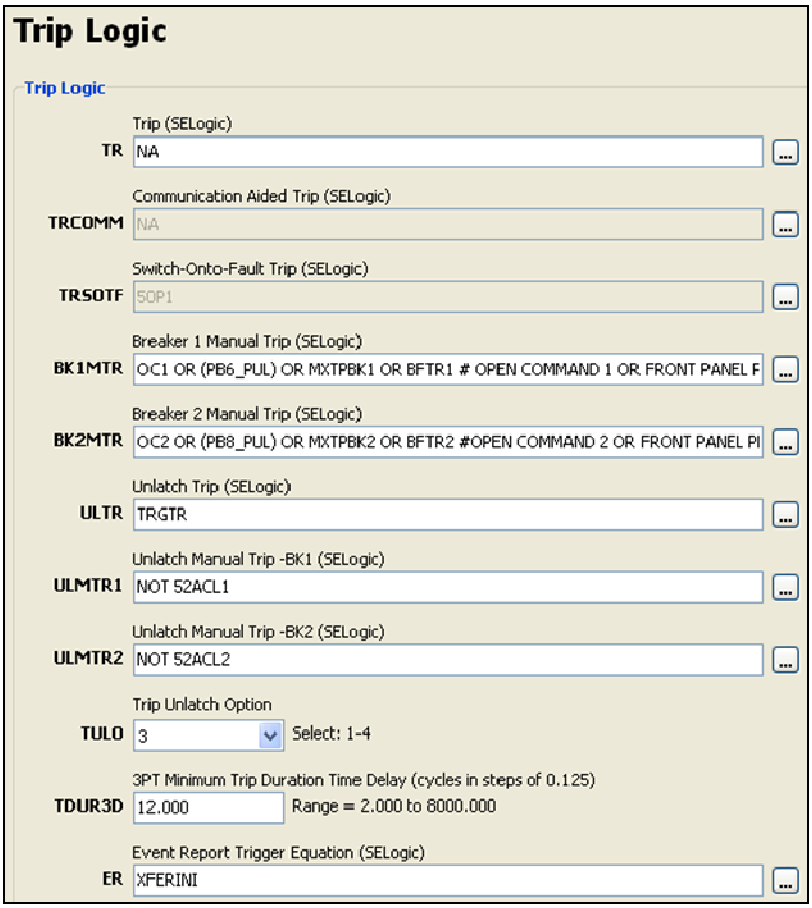

Figure 19 SEL-451 Trip Logic

Close Logic

The internal SEL-451 close logic is programmed as described in Table 24 and Figure 20.

Table 24 Summary of Breaker Close Settings

Name	Value	Description
BKCFD	6	Breaker close failure timer set to twice the closing time of the breaker.
BK1MCL	CC1 OR (PB5_PUL AND NOT MANX_EN) OR CLBK1	Asserts manual closing for Breaker 1 when either a close command for Breaker 1 is issued, the front-panel PB5 is pressed and manual transfer is not enabled, or the close Breaker 1 output from the transfer logic asserts.
BK2MCL	CC2 OR (PB7_PUL AND NOT MANX_EN) OR CLBK2	Asserts manual closing for Breaker 2 when either a close command for Breaker 2 is issued, the front-panel PB7 is pressed and manual transfer is not enabled, or the close Breaker 2 output from the transfer logic asserts.

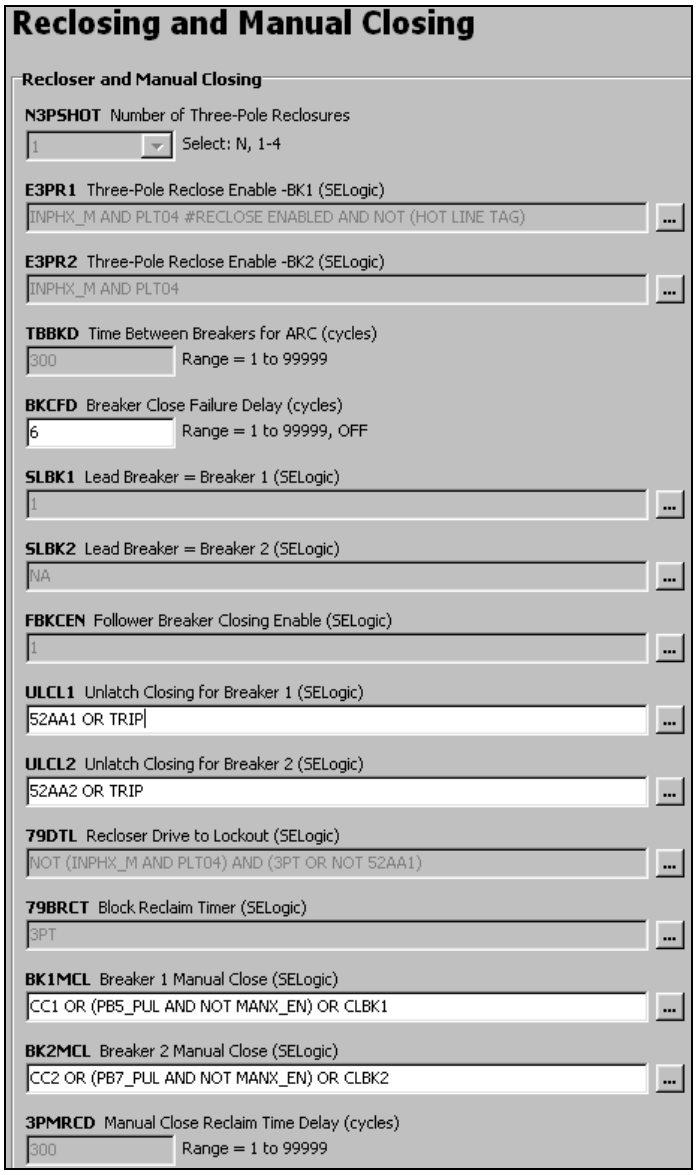

Figure 20 SEL-451 Reclosing and Manual Closing Logic

Breaker Failure

When fast simultaneous transfer is enabled, we strongly recommend applying breaker failure schemes. The SEL-451 provides the functionality. Table 25 includes the pertinent settings for Breaker 1. Similar settings are needed for Breaker 2.

Table 25 Summary of Breaker Failure Settings

Name	Value	Description
EBFL1	Y	Breaker failure enable for Breaker 1.
50FP1	0.5	Breaker failure overcurrent threshold. Follow company practice (however, it is generally set to 10 percent nominal).
BFI3P1	T3P1	Breaker failure initiation.
BFIDO1	4	Breaker failure wait timer. Follow company practice. It is usually set using the breaker open time plus some margin.
BFTR1	FBF1	Breaker failure trip equation.

Outputs

The logic settings for the outputs are described in Table 26. The minimum number of outputs were utilized to implement the scheme.

Table 26 Summary of Output Contact Settings

Name	Value	Description
OUT201	T3P1	Breaker 1 trip signal.
OUT202	BK1CL	Close signal for Breaker 1.
OUT203	RESX_M	Signal to disconnect M3 and M4 when the residual transfer mode is entered.
OUT204	T3P2	Breaker 2 trip signal.
OUT205	BK2CL	Close signal for Breaker 2.

EXAMPLE EVENT REPORTS

The event reports in this section illustrate the operation of the different transfer modes discussed in this application guide.

Simultaneous Fast Transfer

Looking at the digital traces in Figure 21, the FAST_52b and the EXTXINI bits both assert at the same time. Recall that for a simultaneous fast transfer, the trip signal to the source breaker is sent at exactly the same time as the close signal is sent to the alternate breaker. In this particular case, we notice that FASTX (or the fast transfer bit) asserts very shortly after the EXTXINI bit asserts. In this case, the FASTX bit does not wait for the source breaker to open because during a simultaneous fast transfer, both signals are sent simultaneously. Also note that very shortly, less than 1 cycle after 52ACL2 deasserts (the normal source breaker opens), 52ACL1 asserts (the alternate source breaker closes). Having a power source disconnected from the motor bus for less than 1 cycle allows little time for the phase angle and magnitude of the motor bus voltage to

deviate. We can see that at the time the alternate breaker closes (when 52ACL1 asserts), the motor bus voltage, VA, and the source voltage, VS1, are very nearly in phase.

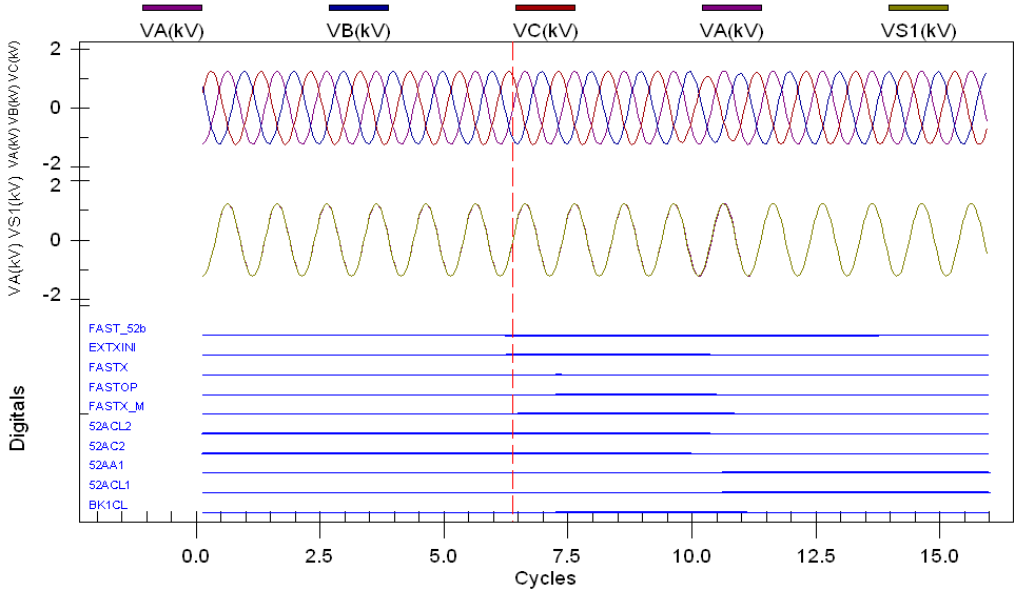

Figure 21 Example Event Report for Simultaneous Fast Transfer

Sequential Fast Transfer

If we compare the example event report for the simultaneous fast transfer shown in Figure 21 with the example event report for the sequential fast transfer shown in Figure 22, we see one primary difference between the two schemes. This difference is that for the sequential fast transfer event, the primary source breaker (52ACL2) opens and then, just over 1 cycle later, the FASTX bit asserts, indicating that the logic waits for the main breaker to open before attempting to close the alternate breaker. The total time for the transfer to occur takes approximately 5 cycles.

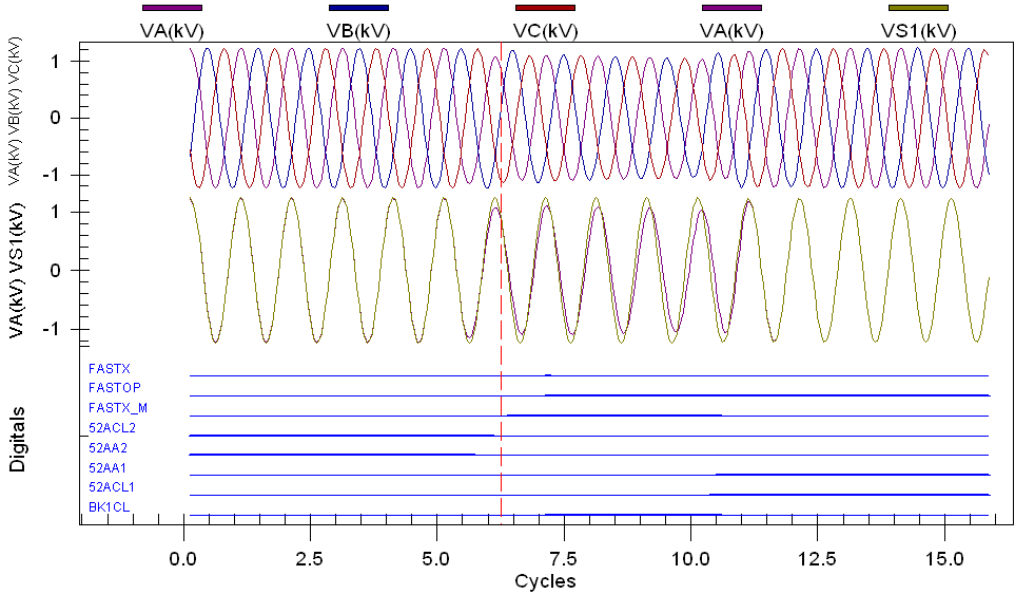

Figure 22 Example Event Report for Sequential Fast Transfer

In-Phase Transfer

For the in-phase transfer, recall that the scheme waits for the phase angle to come completely around 360 degrees, or one slip cycle. We can see from the event report in Figure 23 that this takes approximately 21 cycles to occur. The in-phase transfer logic is able to account for the closing time of the breaker. The IPHXFER bit asserts at approximately Cycle 24 in the event. At approximately Cycle 27 (3 cycles later), the breaker (52ACL2) closes when the two voltages are almost exactly in phase.

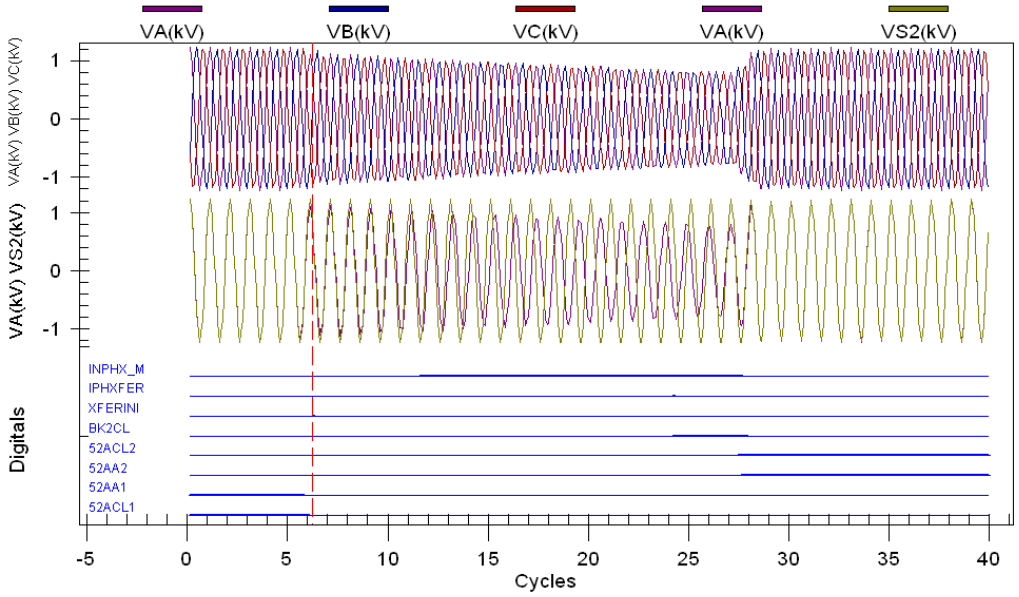

Figure 23 Example Event Report for In-Phase Transfer

Residual Transfer

Recall that residual transfer waits until the motor bus voltage (VA in the oscillograph) falls below a specified level. In this particular event, shown in Figure 24, the alternate breaker does not close until approximately 110 cycles after the primary breaker opens. We can see that in-phase transfer was enabled for approximately 40 cycles during the event report. However, because the motor bus voltage was slipping too quickly, the relay did not allow an in-phase transfer and, as a result, waited for the voltage to decay before initiating a residual transfer.

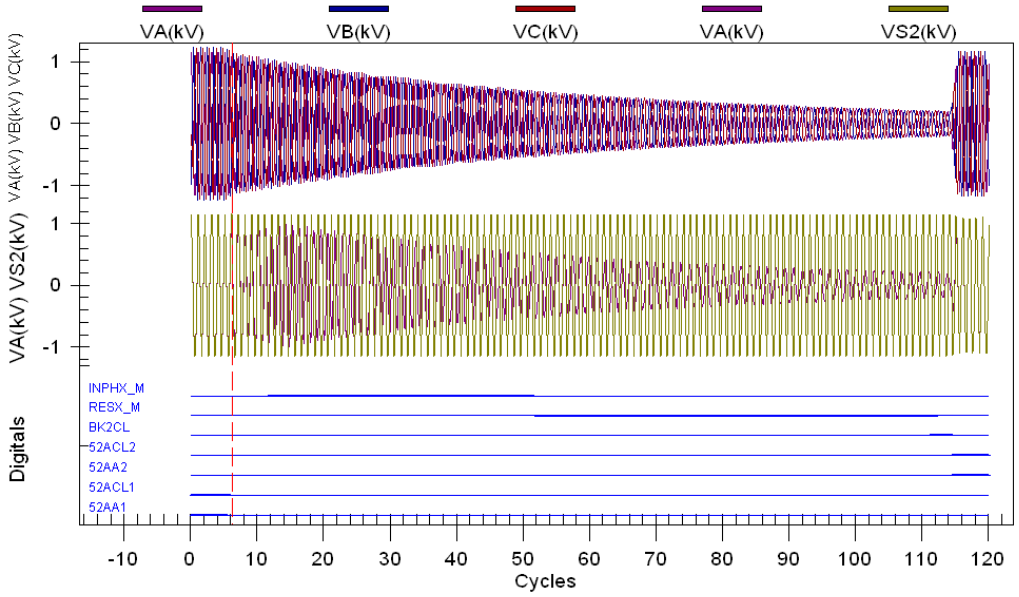

Figure 24 Example Event Report for Residual Transfer

CONCLUSION

This application guide and the accompanying ACSELERATOR QuickSet file provide the settings and SELOGIC control equations necessary to implement a motor bus transfer scheme for a two-source configuration. The logic and settings outlined provide an implementation for fast, in-phase, and residual motor bus transfer. The described settings and logic can be used as is or as a starting point for implementing motor bus transfer schemes.

APPENDIX

This appendix includes a selected portion of the protection SELOGIC control equation and automation SELOGIC control equation settings. The complete SELOGIC control equation settings as well as the other settings are included in the ACSELERATOR QuickSet file that accompanies this application guide.

Protection Logic

```
################################################################################
# MBT ALGORITHM
################################################################################
####################----------SETTINGS----------####################################
XSUP_F := 1 # (XTOSRC1 AND 25A1BK1) OR (XTOSRC2 AND 25A1BK2) # FAST TRANSFER SUPERVISION
XINIBLK := 0 # EXTERNAL TRANSFER INITIATION BLOCK.
EXTXINI := 0 #(PB6 AND 52ACL1) OR (PB8 AND 52ACL2) # (IN201 AND NOT 52ACL2) OR (IN202 AND NOT 52ACL1) #
EXTERNAL TRANSFER INITIATION (FAST 52B INPUT IN IN201/IN202  **FOR EXAMPLE**)
PROTBLK := 0 # PROTECTION TRIP BLOCK.
PSV34 := 0
PSV35 := 0 # AVAILABLE VARIABLES
PSV36 := 0
PSV37 := 0 # >=38 NOT AVAILABLE
####################----------SETTINGS  END----------#################################
```

Automation Logic

```
##########################################################################
# MBT ALGORITHM
##########################################################################
#AUTOMATION LOGIC
####################----SETTINGS-----########################################
#BREAKER CLOSE TIME
T_BKR1 := 6.000000 # BREAKER 1 CLOSE TIME IN CYCLES
T_BKR2 := 4.000000 # BREAKER 2 CLOSE TIME
##########################################################################
#FAST MODE
EFASTTR := 0 #  1 = ENABLED   0 = DISABLED  ********ENABLE FAST TRANSFER MODE ********************
ESIMFX := 0 #  ENABLE SIMULTANEOUS  FAST TRANSFER  1= YES   0 = QUALIFIED TRANSFER
T_FAST := 10.000000 # IN CYCLES - DURATION OF FAST TRANSFER MODE
TDLAY_F := 0.500000 #IN CYCLES - CLOSE COMMAND DELAY AFTER THE MODE IS ENTERED
SVMIN_F := 50.000000 # MINIMUM SECONDARY VOLTS -SOURCE
MVMIN_F := 50.000000 # MINIMUM SECONDARY VOLTS -MOTOR BUS
TSUPU_F := 0.000000 # SUPERVISION TIMER PICKUP
TSUDO_F := 10.000000 #SUPERVISION TIMER DROP OUT
##########################################################################
# IN PHASE TRANSFER MODE SETTINGS
EPHSTR := 1 # 1 = ENABLED   0 = DISABLED *************ENABLE INPHASE TRANSFER MODE*************
MXSL1_P := 20.000000 # MAX SLIP  FOR TRANSFER (HZ) - BREAKER 1
MXSL2_P := 20.000000 # MAX SLIP FOR TRANSFER (HZ) - BREAKER 2
MDSDT1P := 25.000000 #MAX  DSLIP/DT FOR TRANSFER (HZ/SEC) - BREAKER 1
MDSDT2P := 35.000000 #MAX  DSLIP/DT FOR TRANSFER (HZ/SEC) - BREAKER 2
MDVDT1P := -100.000000 # MAX VOLTAGE DECAY  DV/DT FOR TRANSFER (V/HZ) - BREAKER 1
MDVDT2P := -100.000000 # MAX VOLTAGE DECAY  DV/DT FOR TRANSFER (V/HZ) - BREAKER 2
MINV_P := 15.000000 # MIN VOLTAGE MAGNITUDE (SEC VOLTS) FOR DECISION MAKING
T_INPHS := 40.000000 # CYCLES# TIME WINDOW FOR TRANSFER
MXROT_P := 10.000000 # MAXIMUM NUMBER OF ROTATIONS
##########################################################################
#RESIDUAL TRANSFER MODE SETTINGS
ERESTR := 1 # 1 = ENABLED   0 = DISABLED **********ENABLE RESIDUAL TRANSFER MODE**************
TDRES_R := 60.000000 # RESIDUAL MODE TIME DURATION
VMIN_R := 15.000000 # SECONDARY VOLTS# MAX MOTOR BUS VOLTAGE FOR TRANSFER
T_RES := 1.000000 ## TIME DELAY AFTER REACHING THE MAX VOLTAGE.  CYCLES
##############################################################
#EXTERNAL TRANSFER INITIATION
EEXTINI := 0 # 1 = ENABLED  0 = DISABLED  (ENABLES EXTXINI  IN THE PROTECTION LOGIC
##########################################################################
# BLOCK TRANSFER TO SOURCES
BLKSRC1 := 0 # BLOCK TRANSFER TO SOURCE 1  ***  1 = BLOCK  0 = NO BLOCK  **
BLKSRC2 := 0 # BLOCK TRANSFER TO SOURCE 2  ***  1 = BLOCK  0 = NO BLOCK  **
####################----SETTINGS  END -----########################################
```

FACTORY ASSISTANCE

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